Digital interface for quadrature demodulation of interferometer signals[a)]

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We describe a digital interface for processing signals produced by a scanning multichannel far-infrared interferometer/polarimeter for plasma density measurements. The interface samples the interferometer signals in quadrature before digital filtering, demodulation and downloading to a transputer array for real-time tomographic inversion and display. © *1995 American Institute of Physics.*

I. INTRODUCTION

The large amount of diagnostic data generated in fusion experiments often necessitates some pre-processing or condensing of the data flow prior to archiving.[1,2] We are assembling a transputer array for real time tomographic analysis of plasma interferometer measurements on the H-1 heliac[3] at the Australian National University. Aspects of the transputer system are discussed elsewhere.[4,5] In this paper we describe the digital hardware interface for acquisition, demodulation and preprocessing of the interferometer data stream prior to inversion and display by the transputer array. Though designed for interferometry, some features of the interface may be useful in general signal acquisition and phase demodulation applications.

The far-infrared scanning interferometer to be installed on H-1 will provide approximately 100 channels of line-integral density information in six distinct viewing directions of the bean-shaped plasma poloidal cross section.[6] The laser beam is scanned across the plasma by diffracting off the edge of a rapidly rotating disk grating whose grating constant varies discretely with rotation angle.[7,8] Because the beam is also Doppler shifted according to the wheel rotation speed and diffraction angle, the intermediate-frequency (IF) phase-modulated carrier signal is composed of adjacent fringe bursts having discrete carrier frequencies f_n changing in step fashion during the scan over an octave in frequency (typically in the range 10–200 kHz).

Accurate demodulation of such "frequency-agile" signals can pose special problems for standard electronic phase detectors. The interface described here bypasses such problems by synchronously digitizing the interferometer IF signals using a set of fast 12 bit ADCs driven by an external quadrature clock.[9] The quadrature sampling method for phase demodulation (Sec. II) is optimum in the sense that the digitizer needs only sample at twice the information bandwidth rather than at twice the carrier frequency. Moreover, many interferometer channels can be recorded using the same external clock, obviating the need for electronic phase comparators.

Following digitization, the signals are filtered in real-time to remove unwanted noise sidebands. A digital signal processor (DSP) for time-domain filtering of the digitized signal is described in Sec. III. These actions are controlled by a programmable timing interface (Sec. IV) that uses logic state devices and presettable digital counters to regulate the data stream. Results are presented in Sec. V.

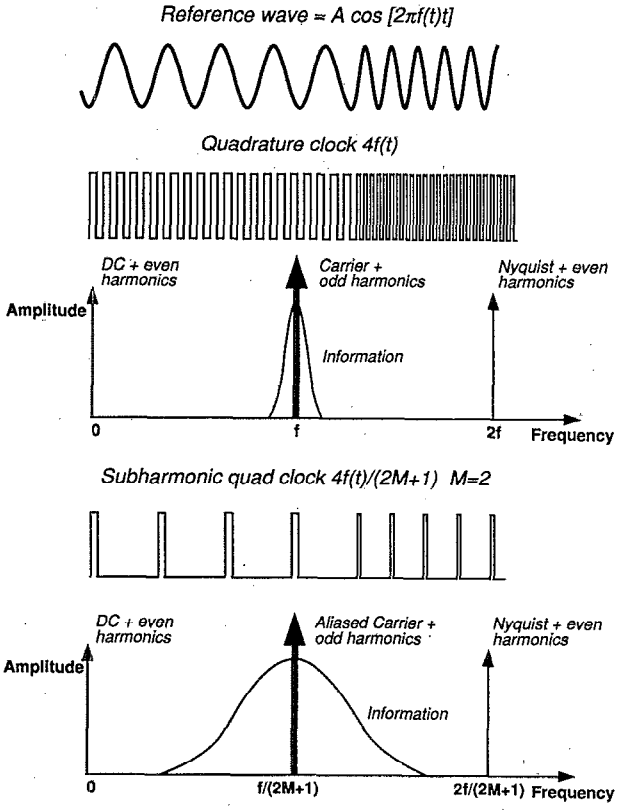

FIG. 1. Pictorial representation of the mapping of time domain information into the frequency domain. When a subharmonic clock is used to digitize the signal carrier, the information bandwidth is increased by a factor $(2M+1)$.

[a)]The abstract for this paper appears in the Proceedings of the Tenth Topical Conference on High Temperature Plasma Diagnostics in Part II, Rev. Sci. Instrum. **66**, 522 (1995).

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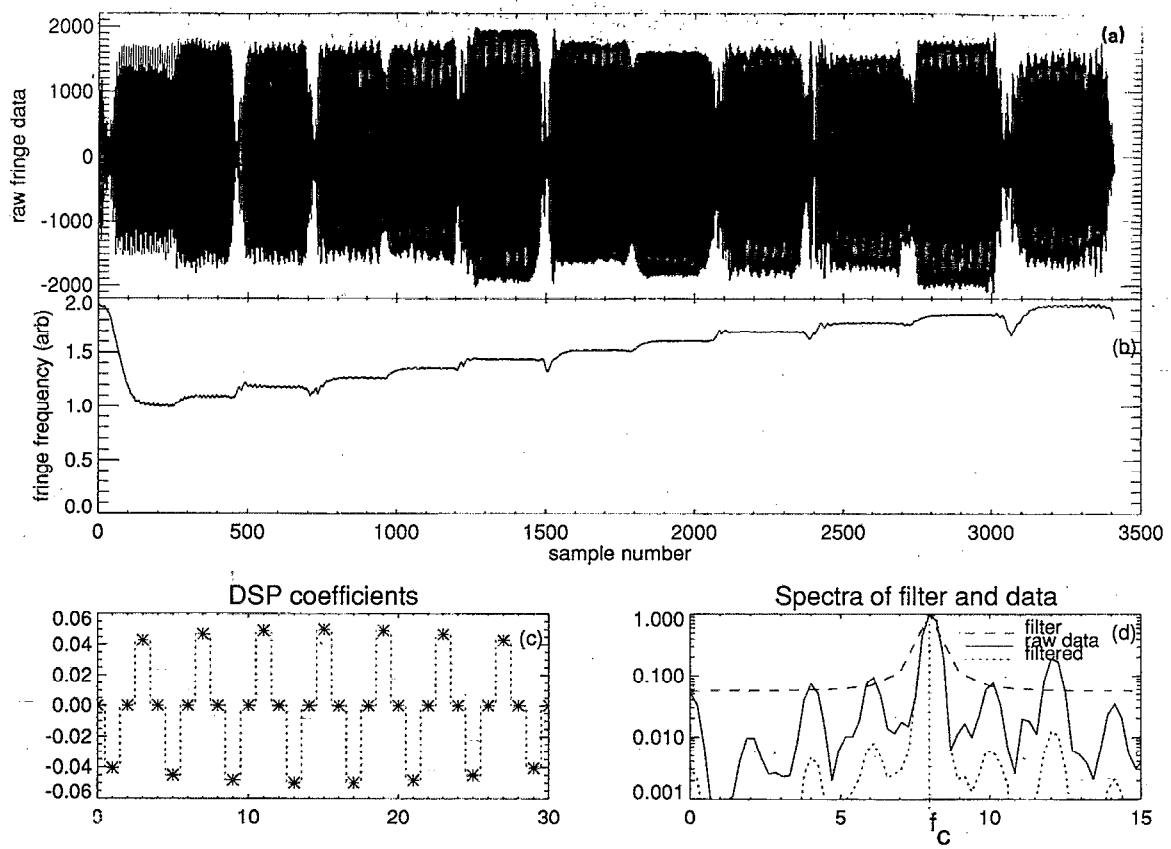

FIG. 2. (a) The synchronously sampled fringes for a complete grating scan, (b) the control voltage to the VCO showing the change in fringe frequency during the scan, (c) rectangularly windowed FIR filter coefficients, and (d) the power spectra for fringe burst No. 1 upon which is superimposed the filter response and the spectrum of the filtered signal showing sideband suppression.

II. SAMPLING DEMODULATION

The sampling demodulation scheme uses clock pulses at four times the carrier frequency $4f$ as an external clock for digitizing the phase modulated carrier. This clock is derived from the reference IF signal using standard frequency synthesis techniques. The ratio of the sampling frequency to the carrier frequency is thus kept constant during the grating scan. The resulting digitized signals are proportional to the cosine and sine of the phase modulation $\varphi(t)$. For high IF frequencies (>100 kHz) it may not be possible or desirable to use a reference clock at $4f$. Indeed, the digitization rate needs to be sufficient only to capture the temporal variation in the phase modulation $\varphi(t)$. This is most easily understood by considering the frequency domain.

For synchronous sampling, the desired components of the discrete Fourier transform of the data samples occupy some interval of the frequency domain around a fixed frequency which we call the "center" frequency f_c. For "quadrature" sampling [rates of the form $f_s=4f/(2M+1)$ $M=0,1,2,...$], the carrier and odd harmonics map to the center frequency ($=f_s/4$), while dc and even harmonics alias to zero and $f_s/2$. It is readily verified that subharmonic sampling ($M\geq 1$) maintains the quadrature phase relationship between adjacent points in the digitized time series, though the fraction of the passband occupied by the phase information increases by a factor $2M+1$ (see Fig. 1). The maximum index M (and hence minimum sampling rate) is determined by the requirement that the information bandwidth not extend beyond the aliasing limits of the sample rate, or the filter passband.

The phase resolution is limited by the digitizer discretization error and noise on the carrier and is insensitive to changes in carrier frequency (within the tracking range of the frequency synthesizer). Small (or transient) phase errors in the phase-locked loop synthesizer can be compensated by digitizing the interferometer reference signal as well as the plasma fringes and subtracting the computed phase angles.

III. TIME DOMAIN FILTERING

Because the ADC sampling rate varies with the instantaneous carrier frequency, the carrier phase is effectively sampled at a constant rate. This is of great importance in our application, as it allows a fixed frequency digital bandpass filter to be applied to the variable frequency data stream. This is accomplished in real-time using dedicated DSP chips (following the ADCs) for time-domain filtering the data stream.

For this real time application, time-domain transversal FIR filters are employed. The synchronously digitized fringe bursts for one complete grating scan as well as the control

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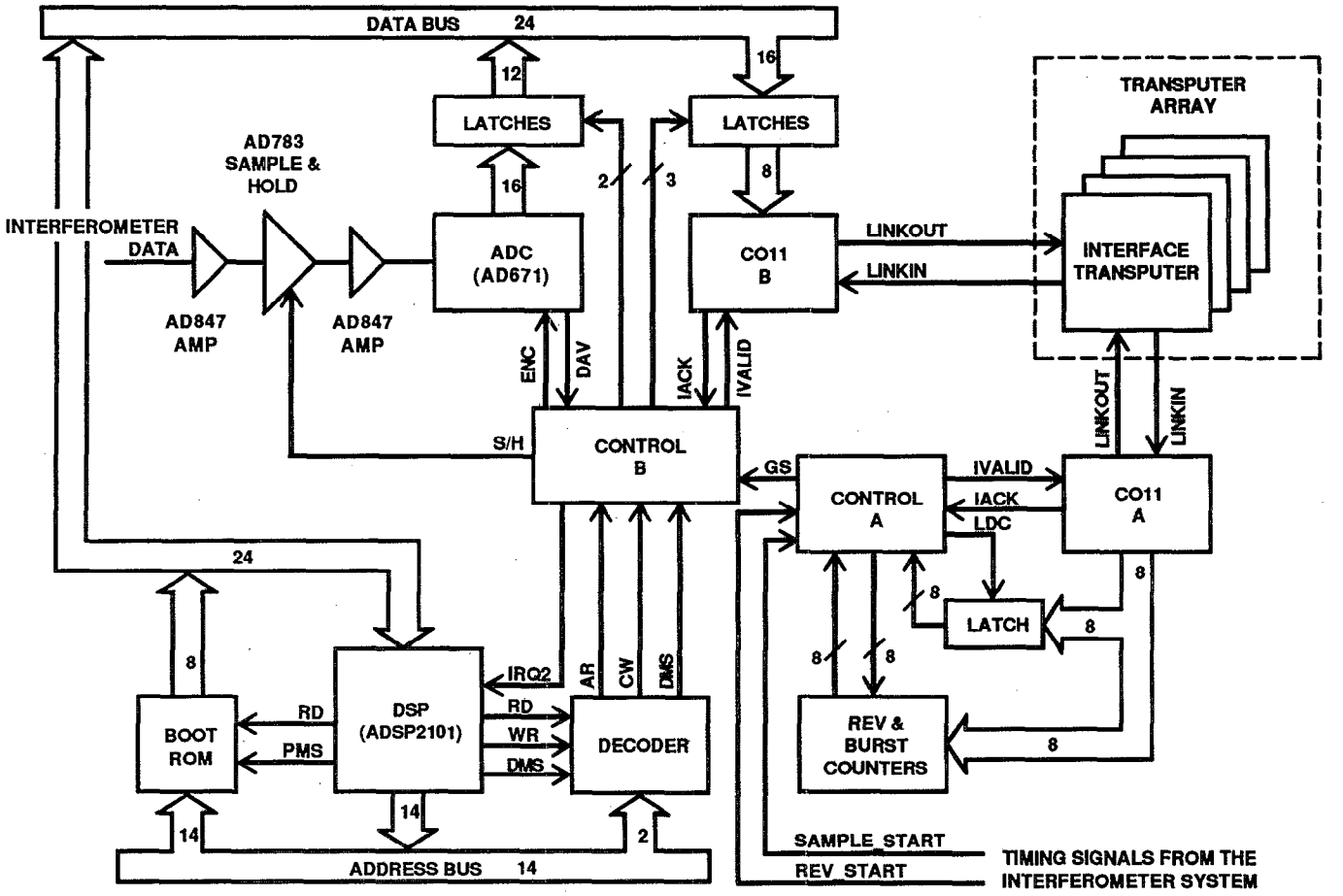

FIG. 3. Block diagram of the digital interface hardware.

signal for the voltage controlled oscillator that tracks the instantaneous fringe frequency are shown in Figs. 2(a) and 2(b). Each of the 12 steps corresponds to a different spatial position within the fan view. A frequency spectrum for one of the noisier fringe bursts is shown in Fig. 2(d). As discussed earlier, the carrier signal resides at the center of the spectrum. The nearby fractional harmonic peaks are caused by parasitic higher-order reflections. The band pass filter about the centre frequency f_c is designed to transmit the phase information from the carrier and eliminate the noise harmonics. Given the sideband levels, a simple rectangular windowed FIR filter [Fig. 2(c)] with a minimum sideband attenuation of 21 dB should be sufficient to bring the signal to noise ratio to about 100:1,[10] while maintaining a relatively fast transient response. If a better sideband attenuation were required, a higher order filter could be used, but the transient response could become a problem as the response time approaches the burst length.

Computer simulations were carried out to optimize the filter design. A 31 coefficient filter with a pass bandwidth of one tenth of the carrier frequency was chosen for the experiments reported here. The filter frequency response is shown in Fig. 2(d), superimposed on the spectrum of the raw data. The spectrum of the resulting filtered data is also shown.

IV. THE HARDWARE INTERFACE

A block diagram of the digital hardware interface circuit for data acquisition and preprocessing for one view of the scanning laser interferometer is shown in Fig. 3. It consists of a fast 12 bit ADC, a DSP (digital signal processing) unit and various control units. Two C011 parallel to serial transputer link adaptors are used to interface through two serial links to the transputer array.

In order to cover the wide range of sampling rates required (from 10 to about 300 kHz), 1.3 MHz AD671 A/D converters, with a maximum conversion time of 750 ns are used. Analogue amplifiers and sample and hold circuits allow the digitizer to track and hold the signals accurately at the carrier frequency.

Single-chip microcomputers optimised for digital signal processing and other high-speed numeric processing applications (Analog Devices ADSP-2101) perform the FIR bandpass filtering. The ADSP-2101 has three computational units, including an arithmetic/logic unit and a multiplier/accumulator ideal for a transversal filter and supports a high degree of parallelism. Provided that the instructions and coefficients are in the on-chip RAM (2K, 24-bit program, 1K, 16-bit data), in one 60 ns clock cycle the ADSP-2101 can perform a multiply/add, generate the next program address, fetch the next instruction, and perform two data moves, up-

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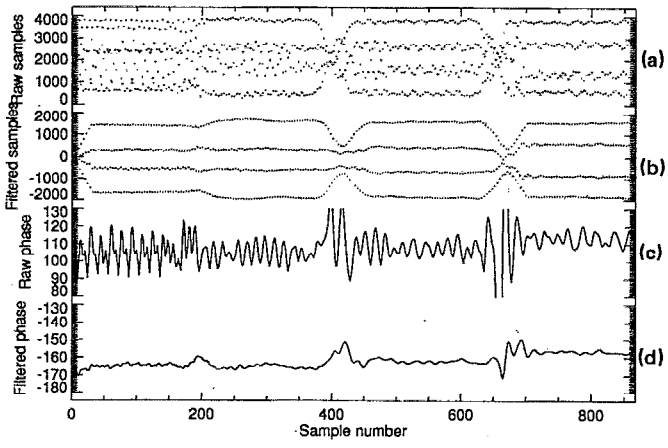

FIG. 4. (a) The unfiltered signal for fringe burst Nos. 1–4, (b) the corresponding filtered signal from the DSP, (c) the unfiltered extracted phase and (d) the extracted phase after DSP filtering.

dating both data pointers. When programmed as a FIR transversal filter, the expected time for an N tap filter to produce a filtered data point is about $N+7$ clock cycles. The ADC (DSP input) and the C011 B (DSP filtered output) are buffered in latches and mapped into external memory in the DSP data address space, and data transfer is interrupt driven.

The interface control units A and B each use two 85C060 16-Macrocell Intel CHMOS EPLDs (Erasable Programmable Logic Devices) operating at 20 MHz clock speed. These programmable logic devices give a degree of flexibility in the design of the interface circuit. For example, the EPLDs in the control unit A together with the counters use the externally supplied $4f/(2M+1)$ clock (START_SAMPLE) and the start scan pulse (REV_START) to control the total number of samples taken during one scan of the rotating grating. The timing parameters are under software control through the transputer and C011 A link adaptor. The EPLDs in control unit B control the ADC sampling and work in conjunction with the ADSP2101 during transfer of the processed data to the transputer through the C011 B link adaptor. Modifications in hardware architecture and timing can be easily performed by reprogramming the logic gates and state machines on the EPLDs.

Filter implementation: The code for FIR filtering is efficiently and concisely expressed in the ADSP assembly language, driven by interrupts for speed and flexibility in buffering. The filter software was developed and debugged with the software simulator (running on an IBM PC or compatible), and hardware debugged and optimized with an "EZ-ICE" in circuit emulator. The filter executable file was programmed into one of the eight 8 kB pages of bootstrap EPROM, which is automatically loaded into on-chip RAM on reset.

V. RESULTS

Figure 4(a) shows the the quadrature sampled unfiltered signal corresponding to the first four fringe bursts of Fig. 2(a). This can be compared with the FIR filtered result in Fig. 4(b). The effectiveness of the filtering is apparent even at this early stage because the undersampling causes the single data stream to appear as four separate traces, two "cosine," and two "sine."

The corresponding extracted phase (arctangent) is more readily interpreted, although this operation (together with the reference phase compensation discussed earlier) is normally performed in the transputer array whose main job is the tomographic inversion of the data.[4,5] Figures 4(c) and 4(d) show the corresponding phases. The filtered signal produces much cleaner phase information and the phase transition between channels is acceptably short for the 31 coefficient FIR filter used.

Processing time is less than 3 μs per sample. This corresponds to the ideal speed of 1 cycle per coefficient, with an overhead of 12–15 cycles for loop initialization, data transfer and some diagnostic I/O. This allows peak fringe rates of up to 300 kHz, or with careful management of input queues in the DSP, average rates of this magnitude. This is more than adequate for the present interferometer, and allows the use of the full sample rate ($M=0$).

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