96 Channel Simultaneous Low Cost Digitizer
ACQ196CPCI

ACQ196CPCI Digitizer Board Specification
96 Channels Simultaneous Differential Inputs, 16 bit 250kSps/channel.
6U, 4HP CompactPCI Data Acquisition Board (single slot)
Flexible Digital I/O Subsystem,
PXI compatible backplane clock and trigger routing
Support for multiple board synchronisation
Intel XScale Microprocessor
Up to 1 GByte of sample memory
PCI 2.2 Interface, 64bit, 66MHz, DMA for max possible PCI bandwidth
64, 32 channels options
100BaseT Ethernet option, port rear RJ45 or PICMG 2.16 Compatible

Description
The ACQ196CPCI board meets the requirement for high channel
density simultaneous data acquisition in cost-sensitve
applications. The board samples 96 input channels
simultaneously with 16 bit resolution at sample rates up to
250kSPS (kilo-samples per second) per channel, while still
offering a robust buffered differential front end input stage with
good AC and DC performance.

Hardware Architecture
The design uses a high performance but cost effective Xilinx
Spartan FPGA to provide an efficient data path to the Intel
XScale microprocessor. This board offers the advanced features
expected of an intelligent board including programmable
triggering, flexible clocking; and a host of data management
functions. Dedicated, high speed Digital I/O allows multiple
boards to be synchronised together for high channel count
applications. The ACQ196CPCI's on board intelligence frees the
host processor from complex real time design issues, allowing
industry standard operating systems to be used in high
performance applications. The board can be configured to
acquire data into a large on-board data store of up to 1 GByte or
to stream the data to an external PCI device.

Software System Support
D-TACQ supports the Linux Operating System and produces full
driver support with source code under GPL. D-TACQ also
provides reference code stubs and application utilities. Drivers for
2.2 and 2.4 series kernels are available. Control of the board is via
simple high level ASCII commands, this is highly scriptable and
has been used with many popular signal processing
environments. Data upload is in raw binary format via DMA on the
PCI bus for maximum efficiency. The onboard embedded system
runs an up to date version of Linux tuned for the ARMV5
architecture, and source code for this is also supplied to
customers on request. The open source embedded system in
combination with the high bandwidth data path offers enormous
scope for application customisation.

Typical Systems
Maximum Channels: conventional Pentium hosted 8 slot
Chassis, up to 7 ACQ196CPCI boards in peripheral mode for up
to 672 channels per chassis. 1200+ channels possible in a 14 slot
bridged backplane chassis

Lowest cost, least space: 1U high, 2 x 6U slot chassis, with 2
ACQ196CPCI boards in standalone mode, avoids cost and heat
load of a conventional Pentium system board, uses standard
ethernet networking to form a compact, robust, diskless
selfcontained data acquisition system: 192 channels in 1U!

Ordering Information
96 Channels with 250kSPS Converters Fitted ACQ196CPCI-96-250
64 Channels with 250kSPS Converters Fitted ACQ196CPCI-64-250
32 Channels with 250kSPS Converters Fitted ACQ196CPCI-32-250
For ethernet append -E
Factory fit with other combinations on request.
Analog Input Subsystem

Analog Input Performance (Typical)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number Of Channels</td>
<td>96/64/32</td>
</tr>
<tr>
<td>Throughput</td>
<td>See Ordering Information</td>
</tr>
<tr>
<td>Resolution</td>
<td>16 bits</td>
</tr>
<tr>
<td>Coupling</td>
<td>DC, Differential Input –</td>
</tr>
<tr>
<td>Sampling</td>
<td>Simultaneous</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>100K (factory option)</td>
</tr>
<tr>
<td>Voltage Range</td>
<td>±10V, ±5V (factory option)</td>
</tr>
<tr>
<td>Common Mode Range</td>
<td>±13V</td>
</tr>
<tr>
<td>Input Voltage Withstand</td>
<td>±100V</td>
</tr>
<tr>
<td>Offset Error</td>
<td>numerical adjust to 0.01% FS</td>
</tr>
<tr>
<td>Gain Error</td>
<td>numerical adjust to 0.01% FS</td>
</tr>
<tr>
<td>INL</td>
<td>± 3 LSBs</td>
</tr>
<tr>
<td>DNL</td>
<td>± 1 LSB</td>
</tr>
<tr>
<td>CMRR</td>
<td>&gt;60dB FS @ 1 kHz</td>
</tr>
<tr>
<td>THD</td>
<td>Target &gt;-80 dB</td>
</tr>
<tr>
<td>SINAD</td>
<td>-90 dB*</td>
</tr>
<tr>
<td>SFDR</td>
<td>100 dBc*</td>
</tr>
<tr>
<td>SNR</td>
<td>86 dBc*</td>
</tr>
<tr>
<td>Full Power BW</td>
<td>250 kHz</td>
</tr>
<tr>
<td>Small Signal BW</td>
<td>2 MHz</td>
</tr>
<tr>
<td>Crosstalk (3 dB)</td>
<td>&lt;90 dB @ 1 kHz FS Input</td>
</tr>
<tr>
<td>Temperature Stability</td>
<td>&lt;25 ppm/C</td>
</tr>
<tr>
<td>INL</td>
<td>± 3 LSBs</td>
</tr>
<tr>
<td>DNL</td>
<td>± 1 LSB</td>
</tr>
<tr>
<td>* Typical values measured at full scale with a 9.76kHz input.</td>
<td></td>
</tr>
</tbody>
</table>

Analog Input Subsystem Block Diagram:
Digital Control Subsystem

Digital I/O

<table>
<thead>
<tr>
<th>Number</th>
<th>Switching Characteristics</th>
<th>Maximum Clock Rate</th>
<th>Minimum High Time for Trigger</th>
<th>Minimum Low Time for Trigger</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>TTL</td>
<td>1 MHz</td>
<td>100 nS</td>
<td>100 nS</td>
</tr>
</tbody>
</table>

The Digital I/Os are used for high-speed control including clocks, triggers and multi-board synchronisation, these are available on the Front Panel, Rear Panel (via the Rear Transition Board) or using PXI compatible P2 backplane routing.

Processor Characteristics

Processor: IOP321 Intel XScale Series I/O Processor
FLASH: 8 MBytes
SDRAM: Standard 200 pin DDR SDRAM SODIMM socket for up to 1 GByte of memory
PCI Interface: 32/64 bit 33/66 MHz compliant to PICMG CompactPCI Specification 2.0 Rev 3.0

On-Board Peripherals

Clock Synthesiser: On Board Clock Multiplication / Division for creation of sample clock from External or Internal Clock source.
10/100 Base T Ethernet: Data and Control port optionally provided through the Rear Panel Transition.
RS232 UART: Console function optionally provided through the Rear Panel Transition.

A rear Transition Module is available providing access to Ethernet and 32 channels of TTL Digital IO.

Digital Control Subsystem Block Diagram
Main Operating Modes

The following paragraphs discuss many of the functions and features of the ACQ196CPCI board. For a complete discussion on the system capabilities please consult www.d-tacq.com.

**Standard Pre / post capture modes**
- Digital and analog threshold and edge triggers.

The transient memory is arranged in a circular buffer with data constantly being acquired until the trigger event. Full flexibility of specification of pre-trigger and post trigger data lengths are available for any length up to the full available fitted memory.

**Generalised Phase Event Mode for maximum flexibility**
- This allows the user to select a trigger event that is either:
  - A Digital Event or a Software Event
  - Either Rising or Falling Edge Digital Event

The user sets up a particular event that initiates the pre-trigger phase, then selects another (or the same) event to move to the post trigger phase. This provides maximum functionality in the data acquisition process including support for initial synchronisation events and for “Gated” trigger behaviour in addition to “Edge” trigger behaviour.

**Sub-Sample Streaming Mode**
- In this mode the board acquires data to a circular buffer as per the Standard Modes but here a subsample of the data is passed to the host in real time to allow the host to monitor real time data. This is especially useful for mixed control/diagnostic applications and for more complex “post mortem” evaluation when the decision to move to post capture is determined by the host. The subsample stream may be made either on the CompactPCI bus or on the local Ethernet if fitted.

**High Throughput Streaming**
- High Throughput Streaming is available when the system designer can allocate the full PCI bandwidth to the ACQ196CPCI digitizer. In this mode the ACQ196CPCI acting as a Bus Master can continuously stream data at at full sample rate on 32bit 33MHz PCI to either host memory or to peripheral storage such as a RAID Disk Array.

**Low Latency Mode**
- In this mode the ACQ196CPCI pushes 1 complete sample worth of memory into host memory to minimise sample latency. This is especially useful in control applications where latency is key. For a typical 32 bit 33 MHz PCI system, all data arrives in host memory in a typical time of less than 12 uS.

**DMA Upload**
- D-TACQ provides a high performance DMA upload feature for the captured Transient data. This allows Data to be uploaded by channel in addition to the entire dataset, sub-sampling DMA is also available.

**In system upgrade**
- The main logic functions are contained in a FPGA (Field Programmable Gate Array) this is loaded by the Microprocessor at power up from the on-board FLASH Memory. The Microprocessor code is also stored in the FLASH Memory. D-TACQ provides utilities for field upgrade of these FLASH programs allowing feature enhancement to be made in the field without a return to base.

**Customisation Potential**
- Most of the main functions of the ACQ196CPCI can be FLASH upgraded in the field; this allows D-TACQ to produce custom enhancements to the board at low cost without extensive NRE development. Potential areas of enhancement are Real Time signal processing with powerful microprocessor / Xilinx co-processor combination, and fast on-board control loops. Please contact D-TACQ if your application requires functionality that is not currently available.

**External Connectors**
- Front panel connectors 3 x 68Way SCSI II sockets for analog signal, 2 x single pin LEMO connectors for external clock and trigger. D-TACQ manufactures a range of compatible signal adapters – Contact D-TACQ Solutions for further information.