Development of a 2000 A DC Current Controller

A thesis submitted for the degree of
Master of Engineering
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by
Chang-Yen Lin

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Statement of Originality

I certify that, except where otherwise acknowledged in the text, this thesis is entirely my own work. I further certify that it contains no material previously submitted for a degree of the Australian National University, or of any other university or tertiary institution.

Chang-Yen Lin
October, 2007
Abstract

A LabVIEW controlled 2000 A DC current controller was developed for more flexible control in the Heliac H-1 fusion plasma experiment at the Plasma Research Laboratory. This current controller consists of two parts, a binary resistor network for coarse-tuning and a PWM current controller for fine-tuning. The effective resistance in the binary resistor network was tested to be within 3% of the nominal values, well within the 5% requirement. A small-scale PWM current converter with the capability to control the current up to 4.3 A was built to verify the theory before the construction of two full-scale PWM current controllers. Each rated at 25 A and 30 A using a FET and an IGBT respectively. A large voltage spike was observed during the turn-off of the solid state switch with a regular RC snubber. After we investigated the resonant response between the stray inductance and the output capacitance of the FET, we introduced an additional RCD voltage clamp snubber, and the voltage spike was reduced by a factor of two. The experimental results of the PWM current controller were in good agreement with the theory.
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Chapter 1

Introduction

1.1 Background

The plasma device, the H-1NF Heliac in the Research School of Physical Science and Engineering provides the opportunity to conduct fusion plasma research. The plasma device is able to generate heat and strong magnetic fields to simulate the physics in the sun. The process requires a reliable and high-power supply to deliver the electrical power for running the plasma device. H-1 is a complicated device that consists of five sets of magnetic windings or coils within its vacuum chamber: the Toroidal Field, Ring Conductor, Outer Vertical Field, Inner Vertical Field and Helical Winding. During plasma fusion experiments, these coils are energized to produce magnetic fields to confine and change the shape of the high-temperature plasma.

1.2 Current Conversion in H-1 Heliac

There are two important parameters in plasma fusion research [5], they are:
\[ \kappa_h = \frac{I_{hw}}{I_{ring}} \]  

\[ \kappa_v = \frac{I_{ov}}{I_{ring}} \]

These parameters are basically the current ratios in coils, used to control the shape of the plasma. There are five separate coil sets, but the machine currently has only two DC converters (main and secondary) to supply the current from 1000A to 14000A. It is too expensive to simply purchase another DC power supply. In many cases coils are in series with each other, and the desired configuration is just a small reduction in one of the coil currents. This may be achieved by diverting some current from a winding by a parallel current regulator. In many cases, a third independently controlled current can be obtained by this technique.

### 1.3  2000 A Current Controller

The prototype 2000 A current controller was designed to meet the following criteria:

1. Rated at 1500 A and can be operated at 2000 A for a short period.
2. Accuracy of 1 A.
3. Maximum current ripple of less than 0.1 A.
4. Capable to extend the operational range of the circuit to allow limited control of the main windings (~20-50mΩ) at currents up to 7000A for short pulses up to 3 seconds.

A first prototype current controller was designed focussing on the characteristics of the Helical winding because it is used most frequently in fusion plasma experiment [5]. A fusion plasma experimental configuration is demonstrated in Figure 1-1. In this experiment, we would like to change the current ratio between the current in the ring \( I_{ring} \) and the current in the Helical winding \( I_{hw} \). As described above, the only way to achieve this without another DC power supply is to employ a shunt circuit in parallel with the Helical winding to divert the unwanted current.
An obvious strategy was to employ a variable resistor across the Helical winding. The department proposed this plan several years ago, to make a water-cooled motor driven rheostat.

![Diagram](image)

**Figure 1-1 Plasma experiment configuration. The shunt circuit diverts the current from the Helical winding.**

The proposed device had two resistive metal tracks made of stainless steel, using a sliding short to change its resistance. Although the idea seemed simple, the plan had never been realized as a result of practical complications. It involved two driving motors, one to drive the short and the other one was used to clamp the sliding contact to the resistive stainless steel tracks to achieve a low resistance contact. This leads to some potential problems:

- A complicated control design and an increased cost; the department was prepared to spend 100,000 AUD on this project (at a rating of 14,000 A) but no company bid on the contract.
- Water cooling is a potential hazard in the laboratory.
- The sliding contact at 2000 A is almost impossible.

Thus the project was abandoned, at least with the requirement to operate at 14,000 Amps.

Current regulation can be achieved using power transistors [4] operating in the linear active region. The power transistors are in parallel with the elements from which the current is required to be diverted. Therefore the current can be easily controlled remotely and the diverted current is dissipated in the power transistors and high-precision power resistors that are in series with transistors. However, this application is difficult to apply in our case because the current is very large (2000 A). It is very expensive and unreliable for such a high current going through transistors.
In order to solve the problem, we decided to use the combination of a passive (resistive) network and a PWM current controller to control the current. The idea was to use an electrically operated mechanical switch (such as a large relay or a contactor) for coarse current control and use a fine tuning element, a PWM current controller, to achieve high resolution current control. This will be explained in chapter 2 at a greater detail.

### 1.4 Thesis Overview

Chapter 2 gives the theoretical background of some relevant technologies, including the binary resistor network and PWM current regulator. Furthermore, we will discuss the methods to protect semiconductor devices, which use RC snubber circuits to absorb transients.

Chapter 3 discusses the design considerations of the binary resistor network. In this chapter, we will talk about the method to calculate the optimum resistance values for binary resistor network and how we decided the parts to purchase by a trade-off between performance and budget. A complete prototype that is controlled by LabVIEW was built. Tests show that it met the required specifications.

Chapter 4 begins with simulations of the PWM current controller using LTSpice and ATP. The simulation results showed a good agreement between theory and simulations. The results from the two simulation programs were compared.

Chapter 5 investigates the full analysis of a small-scale PWM current regulator to check the consistency between real life and theory. This small scale model is rated at 4.3 A and has successfully controlled the current within its rating.

Chapter 6 gives the experimental results of the PWM current controller using two different switching devices, which are FET and IGBT. The current controller initially had an overshoot problem with a regular RC snubber circuit. This problem is lethal to semiconductor devices, particularly FETs, which have relatively less margin for over-voltage than IGBTs. The overshoot is reduced using an additional RCD snubber circuit. A final prototype PWM current converter is built and successfully tested to meet the requirements.

Chapter 7 is the conclusions and the future plans.
Chapter 2

Theoretical Background

2.1 Introduction

The proposed current converter consists of two parts, which are the Binary Resistor Network and the PWM current controller. In this chapter, we will briefly go through basic theory of major components of the proposed current converter and the relevant knowledge, beginning with the binary network and followed by the PWM current controller and methods used to protect it.

2.2 Binary Resistor Network

The binary resistor network is an electrical circuit that has many resistors with their resistance in a binary sequence. The network may be realized in two configurations, the series configuration and parallel configuration. Unlike traditional variable resistors (rheostats), their effective resistances are varied by changing the “On-Off” switching combinations. The series configuration provides a stepwise linear change in the resistance while the parallel
configuration provides a linear change in the admittance. The latter is better suited to high current regulation because the shunt current is shared by the parallel resistors.

Suppose there is a simple binary resistor network with four parallel resistors in pure binary order: R, 2R, 4R and 8R as shown in Figure 2-1. It will have $2^4 = 16$ different effective admittances varying from 15/8R (all switches are closed) to zero (all switches are opened). For example, suppose the network is used to regulate the current from a load with resistance of R (or admittance of 1/R). If the full current is required in the load, all of 4 switches in the binary resistor network will open to have zero admittance, and therefore the current will only flow through the load. On the other hand, if 50% of the full current is required in the load, the switch no. 1 will close to achieve an effective admittance of 1/R, that is the same as the load (admittance of 1/R) to share the current equally.

The possible combinations of effective resistances and admittances of the assumed four-resistor network are plotted in Figure 2-2. Unfortunately, this method has a resolution problem since its total effective resistance is not varied continuously so there will be gaps between them. The gaps are quite significant at high effective resistance due to its binary nature, the worst being 8R-4R = 4R as it can be seen in Figure 2-2. This results in successive current gaps for a given voltage since $I = V / R$.

Figure 2-1 The effective resistance across A-B can be changed by switching operations of the binary network. Thus the current in the load can be regulated.

Figure 2-2 Effective resistance and effective admittance. Note the linear change in admittance and increased gaps in effective resistance.
2.3 PWM Current Regulator

In our application, the PWM current regulator is a Boost Converter, also known as step-up converter, a DC power conversion device that has its output voltage larger than its input voltage. It is mainly used in regulating DC power supplies and regenerative braking in DC motors [1]. The usual applications take advantage of its output voltage. However in this project, we are more interested in the properties of its input stage because the inductor is in the input stage (Figure 2-3), which reduces the input ripple naturally.

![Figure 2-3](image)

Figure 2-3 A schematic diagram of a typical boost converter.

Figure 2-3 gives a drawing of a simple boost converter. Operation of the boost converter is based on the “on-off” operation of the switch, which is also called hard-switching operation. When the switch is closed, the diode is reverse-biased and the output stage is isolated from the input stage, shown in the left hand side in Figure 2-4. The inductor is then “charged” by the input supply. When the switch is opened, the diode is forward-biased and the output stage or the load experiences the energy from both inductor and input supply thus the output voltage is stepped up, shown in the right hand side in Figure 2-4. The switching device works at kilo Hertz range, and for such high speed operations, the switching device is usually a FET or IGBT[1].

![Figure 2-4](image)

Figure 2-4 Right hand side: Switch on. Left hand side: Switch off.
Assuming the output filter capacitor is very large so that the output voltage will be approximately the same, assuming continuous conduction, ignoring the diode forward drop and loss in the FET and inductor, the time integral of the inductor voltage over one time period is zero in steady-state analysis that is shown in Figure 2-5 [1], that is:

\[ V_{in}t_{on} + (V_{in} - V_{out})t_{off} = 0 \]  \hspace{1cm} (2.1)

Dividing both sides by \( T_s \) and rearranging gives

\[ \frac{V_{out}}{V_{in}} = \frac{T_s}{t_{off}} = \frac{1}{1 - D} \]  \hspace{1cm} (2.2)

Where \( D = \frac{t_{on}}{T_s} \) is the duty factor or duty cycle.

Due to power conservation \( V_{in}I_{in} = V_{out}I_{out} \).

\[ \frac{I_{out}}{I_{in}} = (1 - D) \]  \hspace{1cm} (2.3)

Divide equation (2.2) by equation (2.3) gives

\[ \frac{R_{out}}{R_{in}} = \frac{R_{off}}{R_{on}} = \frac{1}{(1 - D)^2} \]  \hspace{1cm} (2.4)

and we obtain

\[ R_{eff} = R_{in} = (1 - D)^2 R_D \]  \hspace{1cm} (2.5)

Figure 2-5 Continuous conduction mode where the inductor current is always greater than zero.
The effective resistance seen at the input terminal can be varied continuously by changing the duty factor. If a small effective resistance is required, the duty factor is increased and vice versa. However, the maximum effective resistance of a boost converter cannot exceed the dump resistor $R_D$. In our application, the boost converter must be working in the “continuous conduction mode” [1], where the inductor current is always greater than zero as shown in Figure 2-5. To achieve this condition, the inductance of the inductor has to be above a certain threshold. The average inductor current at the boundary of this condition is:

$$I_L = \frac{1}{2} i_{L,\text{peak}}$$  \hfill (2.6)

From equation (2.2)

$$I_L = \frac{1}{2} \frac{V_{in}}{L} i_{on} = \frac{T V_o}{2L} D (1 - D)$$  \hfill (2.7)

and

$$I_{in} = I_L$$  \hfill (2.8)

$$V_o = \frac{V_{in}}{1 - D}$$  \hfill (2.9)

Substituting and rearranging equation (2.9)

$$I_{in} = \frac{T V_{in} D}{2L}$$  \hfill (2.10)

$$L = \frac{T V_o D}{2 I_{in}}$$  \hfill (2.11)

The boost converter will operate at the continuous mode if equation (2.11) is satisfied. Low ripple requirement means that the current is in continuous conduction mode for all reasonable currents. The property of the variable effective resistance in the boost converter can be used to fill the successive current gaps in the binary resistor network when it is connected in parallel with the network. In addition, the current ripple due to thermal variation and rectifier circuit in the main can be compensated by use of a feedback control.

Due to its hard-switching operating nature, PWM current converter usually suffers from switching loss. Snubber circuits are usually placed in the boost converter circuit to reduce the effect. A snubber is an electrical circuit that is used to suppress the voltage or current surge during the switching transient or to prevent a false trigger, which might lead to permanent damage to the device.
The over-voltage can be induced during the turn-off of the switching device. The sudden change in the current flow leads to a sharp voltage spike and unwanted ringing. The voltage spike can exceed the $V_{DS}$ rating, which is lethal to semiconductor devices. By introducing a RC snubber circuit, it is possible to minimize this undesired switching effect in semiconductor devices such as FETs and IGBTs. RC snubbers are also used in thyristor circuit for $dv/dt$ protection [1], which prevents false triggering. The common switching devices in PWM current regulators are FET and IGBT because they can work at higher switching frequency to reduce the ripple. Therefore we will only introduce the method to design a RC snubber circuit for over-voltage protection that will be explained in following sections.

### 2.3.1 Snubber Circuit without the Presence of Stray Inductance

The snubber resistor $R_s$ is used to suppress the voltage spike during transition [2].

\[
V_{abs \_ ratings} = IR_s
\]  
(2.12)

\[
R_s = \frac{V_{abs \_ ratings}}{I}
\]  
(2.13)

And

\[
R_s C_s \leq t
\]  
(2.14)

We shall keep the RC time constant smaller than the transient as it is required to absorb the energy from the transient. If the time constant is too large, the voltage across the semiconductor device will rise slowly and results in low efficiency as the energy put into the capacitor is lost. Also, a smaller snubber capacitor helps decreasing the heat dissipation in the snubber resistor because all energy stored in the snubber capacitor is going to be dissipated there.
2.3.2 Snubber Circuit in the Presence of Stray Inductance

There will always be some stray inductances in the circuit. They often resonate with stray capacitances within the circuit and cause ringing and overshoot. In our application, stray inductance cannot be ignored because it is a low voltage and high current application, it has a fast switching frequency to reduce the ripple, and increasing transient losses in semiconductor devices. This makes the stray inductance critical:

\[ V = L \frac{di}{dt} \]  
\[ V \propto L \]  

High switching frequency leads to a large \( \frac{di}{dt} \), to keep voltage low, the inductance has to be low as well. Therefore the series stray inductance must be over-damped [2], that is:

\[ R_s > 2 \sqrt{\frac{L_{\text{stray}}}{C_s}} \]  
\[ C_s > \frac{L_{\text{stray}}}{4R_s} \]

\( R_s \) and \( C_s \) must satisfy equation (2.16) and equation (2.17). The power rating of the snubber resistor also can be calculated assuming RC time constant is significantly smaller than FET rise and fall time because the energy is also dissipated in the switch [2].

\[ W_R = W_{R_{\text{on}}} + W_{R_{\text{off}}} \]  
\[ W_R = \frac{\tau}{\tau + t_{\text{fall}}} W_c + \frac{\tau}{\tau + t_{\text{rise}}} \left( W_c + \frac{1}{2} Ls^2 I^2 f_s \right) \]

Where

\[ W_c = \frac{1}{2} C_s V^2 f_s \]

There are other methods to decrease the switching loss. For example, there is a kind of RC snubbers with a diode in series. By increasing the snubber capacitance, the drain voltage on the FET will rise slower during the turn-off, which reduces the overlapped area with the falling current and thus the power dissipation is smaller but this also decreases the switching efficiency that is not preferred in this project. It is expected that the tailing current is small or will go back to zero before the device is turned off completely.
Chapter 3

Binary Resistor Network Design

3.1 Introduction

A binary resistor network is used to provide a coarse adjustment to the Helical winding, the adjacent current gaps or resolution is aimed to be around 25 A, which can be filled by a PWM current controller. The theory to make a binary resistor network is simple, however it is another story when we deal with a fixed funding in reality. In this chapter, we will talk about how we made the trade-off between performance and budget.

3.2 Design Considerations

The major weakness of the binary resistor network is that its total effective resistance is not continuous, which means there are “gaps” between adjacent binary combinations, leading to a resolution problem. In our assumption, the number of binary resistors should be chosen to have current gaps that are small enough so that they can be filled by the current regulation of the PWM current controller. The adjacent current gaps obviously decrease with increasing
number of switches, which gives a better performance. However, this will not only increase the control complexity but also the cost. Compromises will be made to maximise the performance within the limited budget.

3.3 Network Configurations

There are two major kinds of binary resistor circuits, one using a parallel configuration, and the other uses a series configuration. A large current in any branch is less favoured because parts with high current or power ratings will be more expensive. This is the biggest problem when the series configuration is used because all the current flows through every active branch. Suppose there is a simple series binary resistor network. If we want 500 A of current to flow through the load or Helical winding, the network has to divert 1000 A from the main, which means there will be a huge current (1000 A) flowing through every components in the network. Not to mention the huge power dissipation in the resistors, all the switches that are closed in this operation have to have a current rating of 1000 A, which leads to a higher cost in purchasing switches with higher current rating. Also, the network in series configuration cannot tolerate a single failure in any components.

On the other hand, the parallel configuration is able to share the shunt current, avoiding a large current stream to flow through any single electrical component. In addition, a minor failure in the system is tolerable for the parallel configuration because only some combinations are lost. Therefore the binary resistor network will be using parallel configuration. Considering those constraints that are mentioned in section 3.2, the network will be designed from eight switches in the parallel form.

3.4 Parallel network configuration design

The theory of designing a high resolution binary resistor network in parallel configuration is straightforward, the more switches and binary ordered resistors in parallel, the higher the resolution we have. However, the number of switches is limited to around 8. The challenge is to design a network consist of 8 to 10 switches and results in small current gaps that can be compensated by a PWM current controller within the available budget.
3.4.1 Contactors and Power Resistors

Because of economies of mass production, the most cost effective switches are three-phase contactors. A three-phase contactor consists of three voltage-controlled mechanical switches, which means it has three sets of input and output terminals. This is actually a benefit for us since instead of one big high power resistor, we can use three smaller rated resistors of large resistance value in parallel, leads to easier manufacture. Furthermore, the three individual resistors share more equally in the three-phase contactor.

The resistance of the binary power resistors should be carefully selected so that the maximum current in each branch will not exceed the rating of the switch chosen. Furthermore, large current will result in high power dissipation in resistors, which might require the unnecessary purchase of expensive high power resistors and complicated design of water-cooling system. Water cooling in power resistors was one of our options but it was finally abandoned due to safety issues because the final current controller is going to be placed on top of an 800 V, 14000 A patch panel. (A-Force patch panel)

For high Helical winding current, there is relatively smaller current in the shunt binary resistor network. In this situation, the power dissipation and current are not significant. However, the shunt binary resistor network must carry a large current when it is diverting large current form the source to keep the winding current small. Switches rated at 1000A are very expensive, which are beyond our budget.

In order to solve this financial problem, the current in the lowest resistance branches is limited to values within the ratings of the largest economical contactors, which leads to a higher total effective resistance of the shunt network. This will increase the lower limit of the winding current. It is undesirable because the current regulation range becomes narrower.

This range could be recovered by introducing a small series resistor in series with the Helical winding. However this will also increase the power dissipation and current in the shunt circuit, but it is tolerable for short or pulse-mode operations since switches can take much more current for short period [3]. Furthermore, due to the parallel nature of our binary resistor network, it is always possible to install additional branches that have high-power resistors with ultra low resistances and higher current rated contactors. However, due to time and budget constraints, we are unable to physically construct the additional series circuit and
purchase the additional high-rating parts. This will be possible in the future upgrade plan that will be demonstrated in section 3.4.3.

### 3.4.2 Resistance Selection of Optimum

The resistance of H-1 winding is assumed to be 2.4 $m\Omega$ [6] to calculate the corresponding values for binary resistors because this is the main application for the secondary supply. The binary network would be designed beginning with its least significant bit, which is the resistor with the largest resistance value since we can always get smaller total effective resistance by paralleling two or more larger resistors.

The largest resistance value was estimated based on the Helical resistance and the allowed maximum adjacent current gap, which was decided to be 25A because it is a reasonable rating for the fine-tuning mechanism, the details are covered in chapter 4, 5 and 6. The largest resistance value was decided using simple voltage or current divider law. If we want to divert 25 A from the 1500 A supply, the shunt resistance is:

$$1475 \times 2.4 = 25 \times R_i$$

$$R_i = 142 m\Omega$$

Therefore, in order to divert 25A from the Helical winding, there must be a resistor whose value is 142 $m\Omega$. We used this resistor as the basis and calculated the next resistance by dividing it by 2 each time to get eight resistances in total that are shown in Table 3-1.

<table>
<thead>
<tr>
<th>Resistance ($m\Omega$)</th>
<th>Maximum Current (A)</th>
<th>Maximum Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1 1.1</td>
<td>1028.6</td>
<td>1163.8</td>
</tr>
<tr>
<td>R2 2.2</td>
<td>782.6</td>
<td>1347.4</td>
</tr>
<tr>
<td>R3 4.4</td>
<td>529.4</td>
<td>1233.2</td>
</tr>
<tr>
<td>R4 8.9</td>
<td>318.6</td>
<td>903.3</td>
</tr>
<tr>
<td>R5 17.8</td>
<td>178.2</td>
<td>565.4</td>
</tr>
<tr>
<td>R6 35.5</td>
<td>95.0</td>
<td>320.3</td>
</tr>
<tr>
<td>R7 71.0</td>
<td>49.0</td>
<td>170.8</td>
</tr>
<tr>
<td>R8 142.0</td>
<td>24.9</td>
<td>88.3</td>
</tr>
</tbody>
</table>

Table 3-1 Calculated resistances and ratings.

We simply calculated all possible combinations to simulate the behaviour of this proposed network, which will have $2^8 = 256$ different combinations. The result is plotted in Figure 3-1. It can be observed that the network is capable to regulate the Helical Winding current $I_2$ from
200 A to 1475 A that is represented in blue crosses. The red dots represent the adjacent current gaps, as we can observe, the current gaps are becoming larger at the higher Helical winding current. The largest gap occurs between the last and the second last of the combinations, which is 25 A as we calculated previously. Most of the gaps are smaller than 10 A, which occurs when the winding current is right at the end of the range.

Figure 3-1 Eight resistors give 256 different combinations in total. The successive current gaps become larger as the Helical winding current increases.

These resistance values are sufficient to give a wide range of the current regulation and a good resolution of 25 A. However, this binary resistance combination also gives us high current and power dissipations as shown in Table 3-1. The maximum currents in first three resistors are huge and they dissipate more than 1000 W. The large power dissipations are not such a problem here because the contactors are three-phase, there will be three larger resistors to give the same effective resistance, the power is thus divided by three. However, the maximum current has to decrease somehow because contactors rated at 1000 A are very expensive. Therefore we had to sacrifice resolution or regulating range by limiting current ratings on the proposed network.

Figure 3-2 Price per rated current. The table shows that A75N3 is the best cost to performance ratio contactor in terms of unit rated current, which is rated at 90A per phase, that gives the total current rating of 270A.
We designed the network based on the cost of contactors to keep the cost at the minimum. From Figure 3-2, the analysis shows that A75N3 is the contactor that has the least price per unit rated current, which gives us a total current rating of $90 \times 3 = 270$ A. We have overdriven the current by 20%, which is reasonable if the contactors are working at the room temperature [3]. This condition is guaranteed because the final network will be working in H-1 laboratory, which has good air-temperature regulation.

We limited the maximum current in every branch, so the maximum current flow will not exceed the current rating of the contactors in each branch. The result for simulation of the 320 A limitation is shown in the left hand side of Figure 3-3, which is not acceptable, the regulating range is only from 1000 A to 1500 A. Therefore, we tried the next contactor of the best cost to performance ratio with higher current rating, which is A145N4, $135 \times 3 \times 120\% = 480$ A. The simulation result is shown in the right hand side of Figure 3-3 & Figure 3-2 and is better than 320 A version, the lower winding current limit is down to about 700 A. The result could be better if we use contactors with high current ratings. However, due to budget constraints, we had to work with A145N4 as the highest current rating contactor in the binary network.

![Figure 3-3 The plot in the left hand side shows the simulation result when the current is limited to 320 A. The plot in the right hand side shows the result for current limitation of 480 A, which gives a wider current regulating range. Note here the points that are right on the top (1500A) are because the switches are all disabled (opened), therefore the winding current is at the maximum, that is 1500A.](image)

The resistances had to be adjusted by trial and error to get the best resolution and the widest current regulating range. For example, the big current gap from 880 A to 980 A can be recovered by introducing one more resistor with appropriate resistance value into the network. In addition, we can decrease the maximum current ratings of the resistors by increasing the
resistances for those may have maximum currents that are just above the current ratings of contactors. Their resistances were reduced until they were equal to or slightly below the current ratings of the contactors to utilise the use of contactors. The resistance values for first few high power dissipating resistors, R₁, R₂ and R₃ can be re-calculated based on the maximum allowed current rating in their corresponding contactors, which is 480 A in this case.

Given that the network is in parallel with the helical winding, the maximum current in the next resistor to be added will occur when the shunt resistance is the highest value it attains while that resistor is connected. This only has to be equal to (or slightly less than) the previous value. So we calculate the voltage $V_{N-1}$ for the previous value, and then calculate the next $R$ by $R_N = V_{N-1}/I_{\text{Max}}$. This process is iterated to add successive resistors. We must be sure that $R_N \geq R_{N-1}/2$, which will be true if $I_{\text{Max}}$ is less than 2 times the rating of the previous contactor. We can see from this that it is not clear what the next code after [0 1 1 1 1 1 1 1] is – just that it must start with [1 0 0 0 0 0 0]. It depends on the ratio of $I_{\text{Max}}$ to the current for the previous step. Now the winding current is known, we can find out the voltage across the shunt network, the resistance of $R_3$ is then find out by dividing the voltage by the maximum current rating that is 480 A. This $R_{n-1}$ method is used to figure out $R_1$, $R_2$ and $R_3$.

![Figure 3-4](image.png)

Figure 3-4 The plot in the left hand side shows the maximum current gap is about 20A, the other randomly distributed red dots (current gaps) are caused by transitions between disabled state and re-enabled state due to current limitation of 480A. The plot in the right hand side shows the winding current linearly.

We also made some small modifications to all values to allow some overlap in case that the resistors are not precise values. We had chosen to allow 5% error in the actual resistances. Therefore the final resistances are not in pure-binary order. The details of the final resistances
are shown in Table 3-2. The performance is shown in Figure 3-4, it can be observed that the Helical winding current can be regulated from 420 A to 1500 A with a maximum gap between successive currents of 21 A. The lower limit of the Helical winding current can be further reduced by introducing more MSB resistors into network, which can be done simply in the future if funding is available. The upgrade method is explained in the following section.

<table>
<thead>
<tr>
<th>Resistance (mΩ)</th>
<th>Maximum Current (A)</th>
<th>Maximum Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1 2.8</td>
<td>479.7</td>
<td>652</td>
</tr>
<tr>
<td>R2 3.7</td>
<td>479.6</td>
<td>843.5</td>
</tr>
<tr>
<td>R3 5.0</td>
<td>477.9</td>
<td>1141.8</td>
</tr>
<tr>
<td>R4 9.0</td>
<td>315.8</td>
<td>897.5</td>
</tr>
<tr>
<td>R5 15.7</td>
<td>199.3</td>
<td>622.1</td>
</tr>
<tr>
<td>R6 28.3</td>
<td>117.1</td>
<td>388.8</td>
</tr>
<tr>
<td>R7 50.0</td>
<td>68.7</td>
<td>236</td>
</tr>
<tr>
<td>R8 90.0</td>
<td>39.0</td>
<td>136.6</td>
</tr>
<tr>
<td>R9 166.7</td>
<td>21.3</td>
<td>75.6</td>
</tr>
</tbody>
</table>

Table 3-2 The maximum currents and the maximum power dissipations in all resistors, the maximum currents also represent the corresponding contactor ratings.

3.4.3 Future Upgrade Plan

The network has a regulating range from 420 A to 1500 A with a maximum current gap of 21 A, which is satisfactory for the prototype. It is possible to further reduce the lower limit in future applications. There are two methods, one is to introduce a high power resistor in series with the Helical winding and the other one is to parallel more high power resistors and contactors in the network.

The first method is relatively cheaper and easier to upgrade the system. In order to widen the regulating range, we can plug a resistor in series with the Helical winding using the plugs and sockets on the “A-Force” patch panel when low Helical current is required. When an extra resistor is in series with the Helical winding, the effective resistance of the Helical winding is increased while the resistances provided by the shunt network remain the same. Therefore there will be more current flowing through the shunt network, and the lower limit of the current regulating range is decreased. On the other hand, the extra current flowing through the shunt network might kill the contactors and resistors. Therefore it is not recommended to be used in continuous-mode operations but it is still workable in pulse-mode operations [3].
The other method is more expensive but will be able to provide continuous-mode operations. The method is to parallel more branches that consist of higher current rating contactors and resistors with lower resistances in the shunt network. Therefore the upgraded shunt network can provide a smaller total effective resistance and achieve a wider range of current regulation. Also, unlike the previous method that requires electricians to install the cable when low Helical winding current is needed, the upgraded network will still be fully automatically controlled in whole current regulating range.

### 3.4.4 Purchase Lists

Since contactors are three-phase, the resistors with three times resistances were purchased so that we have the equivalent resistances as we calculated in the previous section when they were paralleled.

<table>
<thead>
<tr>
<th>R</th>
<th>Resistance ($m\Omega$)</th>
<th>Power Rating (W)</th>
<th>Number Ordered</th>
<th>Unit Price</th>
<th>Price</th>
<th>Effective Resistance ($m\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>R1</td>
<td>8.5</td>
<td>217.3</td>
<td>3</td>
<td>$300</td>
<td>$900</td>
</tr>
<tr>
<td></td>
<td>R2</td>
<td>11</td>
<td>281.2</td>
<td>3</td>
<td>$300</td>
<td>$900</td>
</tr>
<tr>
<td></td>
<td>R3</td>
<td>15</td>
<td>380.6</td>
<td>3</td>
<td>$300</td>
<td>$900</td>
</tr>
<tr>
<td></td>
<td>R4</td>
<td>27</td>
<td>299.2</td>
<td>3</td>
<td>$300</td>
<td>$900</td>
</tr>
<tr>
<td></td>
<td>R5</td>
<td>47</td>
<td>207.4</td>
<td>3</td>
<td>$300</td>
<td>$900</td>
</tr>
<tr>
<td></td>
<td>R6</td>
<td>85</td>
<td>129.6</td>
<td>3</td>
<td>$150</td>
<td>$450</td>
</tr>
<tr>
<td></td>
<td>R7</td>
<td>150</td>
<td>78.7</td>
<td>3</td>
<td>$100</td>
<td>$300</td>
</tr>
<tr>
<td></td>
<td>R8</td>
<td>270</td>
<td>45.5</td>
<td>3</td>
<td>$100</td>
<td>$300</td>
</tr>
<tr>
<td>LSB</td>
<td>R9</td>
<td>500</td>
<td>25.2</td>
<td>3</td>
<td>$100</td>
<td>$300</td>
</tr>
</tbody>
</table>

Total Cost $5,850.00

Table 3-3 Purchase list of Power Resistors.

<table>
<thead>
<tr>
<th>ABB Contactor</th>
<th>Current Rating Per Phase (A)</th>
<th>Total Current Rating with 20% Overdrive (A)</th>
<th>Number Ordered</th>
<th>Unit Price</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>A145N4</td>
<td>135</td>
<td>486</td>
<td>3</td>
<td>$286</td>
<td>$858</td>
</tr>
<tr>
<td>A75N3</td>
<td>90</td>
<td>324</td>
<td>2</td>
<td>$190</td>
<td>$380</td>
</tr>
<tr>
<td>A50N2</td>
<td>45</td>
<td>162</td>
<td>2</td>
<td>$110</td>
<td>$220</td>
</tr>
<tr>
<td>A16N0</td>
<td>18</td>
<td>65</td>
<td>2</td>
<td>$80</td>
<td>$160</td>
</tr>
</tbody>
</table>

Total Cost $1618

Table 3-4 Purchase list of three-phase Contactors.
3.5 Final Prototype Binary Resistor Network

We were only able to assemble the least rated binary branches with four largest resistance values (500 $m\Omega$, 270 $m\Omega$, 150 $m\Omega$ and 85 $m\Omega$) because the manufacturer was only confident with them. The manufacturer had no experience in making power resistors with such small resistance values, especially 8.5 $m\Omega$. We had to check and test the resistors with smaller power rating before we go onto high current. In fact, we spent a few months to persuade the manufacturer to make such low resistance power resistors for us. We did not want to scare the manufacturer away because they are probably the only one who is able to make power resistors with small resistance values in Australia. This delayed the ordering process so we did not have enough time to assemble all of them. However, assembly of the four least rated binary branches still proved the theory.

We assembled the resistors and contactors and fixed them onto a MDF (medium density fibre board). Then we used the largest copper wire suggested in the datasheet of ABB contactors [3] to minimize the resistance in the wire. 25 $mm^2$ and 16 $mm^2$ wires were used for A50 and A16 respectively. The wires are supposed to be as short as possible, however we had to keep about 20 cm of wire between resistors and contactors to ensure the heat does not transfer so quickly from power resistors to contactors. This is important because the rating of contactors is inversely proportional to their temperature [3].

![Figure 3-5 Measured resistance and admittance. The solid lines are the theoretical values. The crosses are the measured values.](image)
We used LabVIEW to control the binary resistor network. The LabVIEW breakout box cannot provide enough power to control the contactors directly. A transformer was required to power them up. Solid-state relays are used between the contactors and the transformer as the control medium, which are connected to the LabVIEW breakout box.

A 300 VA transformer was used, which is powerful enough for all contactors to hold at steady-state but it is relatively too small for nine contactors pull in or pull out at the same time. Therefore we programmed a 10 ms time delay between operations of the contactors to decrease the peak current drawn by contactors. It is not critical now because these four contactors we are using are small, they do not require a large current to drive the coils inside them. However when we install the large contactor, such as A145, it will need 20 A to pull in. There are three A145 in total and a peak current of 60 A, which is well beyond the rating of the transformer. The final prototype of the binary resistor network is shown in Figure 3-6.

The effective resistances were measured from the network’s input terminal (indicated in Figure 3-6 as blue circles) to ensure their accuracy, including the resistance contributed by the contactors and the wires. The effective resistances are all within 3% of the nominal value, well within the requirement of 5%. Therefore there should not be any unexpected current gap. The measured resistance and the admittance are plotted in Figure 3-5. The increase in admittance from binary code 7 to 8 is deliberate, and was designed to make the network tolerant of variations in resistance of up to 5%. As this was by far the lowest set of resistance values the manufacturer (Hurtle-Webster, Tyabb Vic.,) had made, 5% was the tightest tolerance they would agree to supply. In practice, the resistance values were more accurate than this by about a factor of two.

We wrote a LabVIEW program to control the binary resistor network. We created a look-up table that contains $2^4 = 16$ binary combinations and their corresponding effective resistances. The program searches for the optimum binary combination that is the closest above the required resistance. Therefore the effective resistance can be reduced by the PWM current converter that is parallel with the network in the future. Note here, the total effective resistance can only be less when paralleling another resistive element. That is the reason why the program selects a larger value than required. When a correct binary combination is selected, the program will turn on or turn off the contactors in a sequence with 10 ms delay. We have to turn off the input power to the binary resistor network manually before we do any change to it because this would create arc and damage the contact within the contactors.
3.6 Conclusions

We successfully designed a binary resistor network that is able to achieve a wide range of current regulation from 420 A to 1500 A. It is flexible for future upgrade to make the network capable for current regulations lower than 420 A. The maximum successive current gap is 21 A that is reasonably small and can be compensated by the PWM current controller, which will be covered in chapter 4, 5 and 6. Due to safety and time constraints, we were only able to assemble four binary branches. However, the test results agree with the theory that can be applied to the rest of the binary branches.
Chapter 4

Simulations

4.1 Introduction

ATP and Spice are the two most widely used simulation programs [1]. They both have advantages and weaknesses. In this chapter, we will use both programs to model the PWM current converter and compare them.

4.2 ATP Simulation

ATP (or the commercial version “EMTP”) is a commonly used circuit simulation program, which was used to demonstrate the possibility of boost converter to regulate current first. We met some difficulties of using ATP to simulate the converter due to ATP’s fixed step size, trapezoidal integration method [1]. Because the trapezoidal method effectively averages two time steps, around the transition from open to close, effectively the diode and the switch are both closed for part of a computational cycle. In other words, the switch is closed while the diode is not quite opened at the time step and this forms a short circuit loop. When this
situation occurs, the stored energy in the capacitor C is significantly decreased because a large current flows. This problem can be easily reduced by decreasing the time step. However, this reduction is only first order in step size, and will lead to a heavy computation load.

Figure 4-1 The boost converter circuit diagram created using ATP.

In order to solve the problem, we placed a small stray circuit inductor $L_2$ in series with the diode to prevent the electrical energy loss (Figure 4-1). The inductance should satisfy $LC$ time constant, $\sqrt{LC} \gg \Delta t$ where $\Delta t$ is the time step. The required inductance was calculated to be at least orders of ten of 10 nH. In fact, the addition of this inductance is making the simulation closer to real life because the real diode is not just simply a switching device that is able to stop current flow immediately when it is reverse-biased or to let the current flow when it is forward biased. The injection of minority carriers at the beginning of the conduction period can be approximately modelled as an inductor. A reverse current flows for a short period of time due to its “stored charge”, which is swept out to block the negative voltage. The removal of the stored charge is like a capacitor. We could place a capacitor in the circuit to make the model more realistic. For this work, the result of the ATP simulation is acceptable.

Figure 4-2 The output voltage drops rapidly over a short period without the presence of the inductor $L_2$. The voltage of the model without the series inductor only reaches 1.3mV while the other model reaches 1.8mV. There is a significant voltage difference between these two models, which is 0.5 mV or 25% after two periods.
The RC snubbers were calculated using the method in section 2.3.1 and section 2.3.2, the snubber resistance and snubber capacitance are 10Ω and 0.1μF. Rather than attempt to examine voltage and current waveforms for every capacitor and inductor, we checked for this type of numerical error based on energy conservation. We then performed the energy conservation test on the model comparing input power and output power, which was to sum up all possible power dissipation and compare with the input power. The total parasitic power loss (losses in parasitic resistances) was 6.2% of the total power 1.69W. Also, by taking the parasitic loss into account, more than 97% of power was conserved, which is acceptable in simulation. Note that efficiency is not an important issue for this project because the converted power is dissipated in any case.

![Figure 4-3 A result of ATP simulation. The input current (red) is 0.8A when duty factor is 0.5. The switching signal (pink) is generated by the sawtooth signal (blue) and its set point (green). Note there is a small ripple in the input current. The effective resistance is calculated as 2V/0.8A=2.5Ω.](image)

### 4.3 LTSpice Simulation

LTSpice is a spice simulation program licensed by Linear Technology®, an integrated circuit manufacturer. It has an advantage over ATP, it has many built-in real components, making circuit simulations closer to real life. For example, ATP does not have real FETs or IGBTs, we had to replace them with a controlled switch. On the other hand, LTSpice has more than 20 different FETs and IGBTs that are actually commercially available to use, and accepts various types of Spice models and sub-circuits.

Unlike ATP’s fixed step size, trapezoidal integration method, LTSpice will precede extremely small time steps when a sudden discontinuity is detected. It might result in a problem of convergence at the worst situation. However it had never been observed when a RC numerical snubber circuit with the values calculated using the method mentioned in section 2.3.1 was
used across the switching devices in our simulations. This property makes the software easier to use. However it should be noted that by the time LTSpice was used, the models had been developed to a point where sufficient parasitic components had made the analysis of the circuit less critically dependent on integration parameters.

![Figure 4-4 The boost converter circuit diagram created using LTSpice.](image)

We built a boost converter model using LTSpice, the circuit diagram is shown in Figure 4-4. The efficiency between input and output can easily go to 90% without putting any extra stray components.

![Figure 4-5 A plot shows the results of LTSpice simulation. It can be observed that there are more data points in the transitions, which confirms the program has reduced the step size.](image)

### 4.4 Conclusions

We encountered some difficulties in ATP simulation due to its fixed step size, trapezoidal integration method. However this should not affect the real life experiment as long as we have a snubber circuit in parallel with the switching elements. On the other hand, LTSpice is more suitable in circuit simulation, especially solid state power electronics while ATP is generally used in AC power system simulations, and is particularly flexible in modelling feedback controllers. Therefore LTSpice is used to model the power semiconductor circuits in the rest of the thesis.
5.1 Introduction

A smaller version of the boost converter was built using lower rated components to measure and understand real-life properties of the boost converter. It was an opportunity to examine the consistency between theory and reality. This also minimized the chance of destroying expensive full-scale parts accidentally in the future.

5.2 Experiment Setup

The switching signals for the Boost converter were generated by TL494, a PWM power supply controller, which provides 0% to 90% of duty factor at the Pull-Down operation using sawtooth modulation [11]. The switching frequency was set to be 20 kHz. Although the Push-Pull operation that provides an equal rise and fall time in the output switching signal was preferred, it was not used in this experiment because the range of the duty factor is decreased by half in this operation (0%~45%).
A power MOSFET (IRFZ44N) was used as the switching device for the small-scale boost converter. It has the current rating of 49A and Voltage rating of 55V. According to the theory, the output voltage is larger than the input. Due to energy conservation, the output current decreases as the output voltage increases. Therefore, we were more concerned about the voltage rating here. The input voltage was then chosen to avoid over-rating operation. The output voltage is greatest when duty factor is at the maximum, which was limited to 90% in TL494. From equation (2.2):

\[
V_{in} = V_{out} (1-D)
\]

\[
V_{in} = 55 \times (1-0.9) = 5.5V
\]

The input voltage should not exceed 5.5V to avoid damage to the power MOSFET. The input voltage was then chosen to be 5V to have some safety margin. A heat sink was provided on the power MOSFET to minimize the chance of over-heating.

An inductor with a large inductance is preferred because it directly determines the input current ripple:

\[
V = L \frac{di}{dt}
\]

\[
V = L_{f,m} \frac{di}{D}
\]

For a fixed input voltage, the change in current or current ripple is inversely proportional to the inductance. The inductance of the available ferrite cored inductor was measured to be 5mH. For switching frequency of 20 kHz, an input voltage of 5V and a duty factor of 50%, the ripple in the input current was calculated to be 25mA using equation (5.2). This is a factor of four better than required.

There is a disadvantage to using a ferrite core because it saturates as the inductor current increases. An air cored inductor will be used in the future full-scale boost converter, therefore saturation should not be a future concern although achieving a large enough inductance will be a problem. The saturation current was calculated by the following:

\[
B = \frac{\mu_e NI}{L_{eff}}
\]

\[
L_{eff} = \frac{L_f}{\mu_f} + \frac{L_{gap}}{1}
\]
Where $B$ is the magnetic field, $\mu_0$ and $\mu_f$ are the permeability of the vacuum and the ferrite respectively, and $N$ is the number of the turns of the inductor. The inductor saturates when inductor current is around 3A. This estimation only gave us a very rough answer because we had limited information about the inductor that we were going to use. The real saturation current for this inductor was measured in the experiment. According to the wire diameter in this inductor (~1mm), its steady state current rating is around 1.6A. We considered inductor itself as a heat sink since it has a considerable mass, so that we used currents about twice this size for short periods of time.

The input current rating was chosen based on this because current ratings of other components were all greater than 3 A. The heat dissipation in the inductor became a problem because the heat was trapped in the inner part of the winding. Since we were short of inductors with higher current rating, we just had to be careful at the high input current. This was achieved by careful monitoring of the inductor temperature, avoiding the operation at high power and freezing the oscilloscope when taking data at high duty factor.

The input current was determined by the input voltage and the effective resistance of the boost converter as seen from the input terminal in equation (2.5). According to equation (2.3) and equation (2.5), the input current is at maximum when the effective resistance is going towards the minimum that corresponds to large duty cycle. The effective resistance can vary from $R_D$ to $0.01R_D$ as the duty factor is changed from 0% to 90%. The parasitic resistance must be taken into account especially when the effective resistance is small in high duty factor because it will become comparable to the effective resistance itself. The major parasitic resistance was contributed by inductor, which was measured to be around 1 $\Omega$. Thus:

$$\frac{5}{R_{\text{eff}}} \approx 3.3A$$

(5.5)

$$\frac{5}{R_D (1-0.9)^2 + 1} = 3.3$$

(5.6)

$$R_D \geq 50\Omega$$

(5.7)

Therefore the power dumping resistor had to be at least 50 $\Omega$ to ensure the input current does not go too high.

We have a greater interest in input characteristics of the boost converter. One of the important input characteristics is the input current ripple that should be as small as possible. The input
current ripple is minimized using a high inductance inductor. On the other hand, the output ripple has to be controlled to avoid excessive voltage on the FET. In the steady-state analysis in chapter 4, the capacitance of the output filter capacitor was assumed to be large so that the output voltage stays constant. All formulae were derived based on this assumption. The filter capacitor not only keeps the output voltage ripple small but also prevents large voltage surges that will damage the FET at switching transitions induced by \( V = L\frac{di}{dt} \). Its value should be large enough to ensure the RC time constant is significantly larger than the switching period to decrease the output ripple. We chose a common capacitance value, which was 470 \( \mu F \). The RC time constant was then \( 470 \times 10^{-6} \times 50 = 23.5ms \) that was significantly greater than the switching period \( 1/20kHz = 50\mu s \) to ensure a small output ripple.

The diode, a Schottky rectifier (12CTQ45), was used to separate the input and output stages of the boost converter. The filter capacitor will be ineffective without a diode because the energy stored in the filter capacitor will flow back through the turned-on FET rather than the dumping resistor. The fast Schottky diode was used because it has a fast switching characteristic, which results in less switching loss in high frequency operation, and a low forward voltage.

The values for RC Snubber were calculated using the method in section 2.3.1, which were 10 \( \Omega \) and 100 nF.

### 5.3 Experimental Results

**Figure 5-1** The output voltage increases as expected, however the efficiency drops dramatically as the duty factor goes up.
The agreement between experiment and equations is good at small duty factors. Theoretically, the output voltage should be increasing towards infinity as the duty factor is approaching unity. However this is not true due to the existence of parasitic elements in real life. In Figure 5-1a, the difference between theoretical and experimental values is getting larger as duty factor increases, which indicates the lowered efficiency in high duty factor. The major parasitic elements of the boost converter are switching loss in FET, inductor loss and diode loss.

Figure 5-2 Switching waveforms at DF = 60.8%. Significant power dissipation can be observed during switching. The voltage falls a factor of two faster than it rises, therefore the time scale of falling transient loss is twice as fast than the rising one for easier viewing.

We used a Tektronix AC current probe to measure the current, which must have an average of zero current over time period. This caused an undesired off-set on the oscilloscope display when we measured DC current. Therefore we used excel to correct this off-set by introducing a correction factor, so that the current is exactly zero when the FET is in the off state.

In theory, MOSFET will turn on or turn off immediately as soon as the gate voltage goes above or below the threshold, which will not result in transient loss. In fact, the voltage
and the current take time to rise or fall. The overlapping period results in power dissipation. An example of transient loss is given in Figure 5-2, a significant power loss is observed before and after the MOSFET is fully turned on and turned off. The rise time is about twice longer than turn-off time in the experiment, which are 225 ns and 126 ns respectively. This is because the divider circuit configuration is active “pull-down”, which is demonstrated in Figure 5-4.

![Diagram](image1)

**Figure 5-4** The switching circuit is shown in the top. When M2 in TL494 chip closes, the MOSFET closes and experiences an effective gate resistance of 50 Ω. When it is off, MOSFET experiences a gate resistance of 100 Ω. This explains the difference in rise and fall time.

The effective turn-on gate resistance is a factor of two larger than the turn-off resistance and the time constant is $\tau = RC$, therefore the time it takes to turn off will be approximately the factor of two faster than the turn-on time if we assume the effective capacitance at the gate terminal is constant. This is not true in practice but is a reasonable approximation in that the charge required to turn the FET on is approximately equal to opposite to the charge required to turn off. This phenomenon leads to greater power dissipation in turn-on than in turn-off, which is shown in Figure 5-3. In this case, the dominant loss in MOSFET is the conduction loss, which is caused by the drain to source on-resistance. In Figure 5-3, the conduction loss is dominant over transient losses.

![Graph](image2)

**Figure 5-5** Diode loss and inductor loss. Note the inductor loss is large, it reaches 0.9W at DF = 92.3%.
The switching loss of the diode was not measured because the diode is a Schottky rectifier, which has fast switching characteristics and virtually unmeasurable switching loss, therefore only conduction loss is measured in this experiment. The diode power dissipation is small compared to other losses because the diode current is smaller than those in other components. The boost converter steps up the input voltage into a larger output voltage therefore the current in the output stage has to be small for energy conservation, leading to a smaller loss.

The inductor loss is most significant in this experiment because it has a big stray resistance of 1 Ω. As the inductor current increases, the power dissipation increases in proportion to the current square. The power dissipation at high duty factor was so large that it overheated the inductor during the experiment, which increased the stray resistance and produced more heat. We had to take the measurement fast before the resistance was increased. The only way to solve this problem is to use inductors with higher current ratings.

The efficiency between input and output drops to 30% at the maximum duty factor Figure 5-1b, which is not desirable for commercial use. However it will not affect our system as long as power dissipations are below ratings of all those components because we meant to dissipate the power anyway, it does not matter whether it is dissipated in the dump resistor or other components. The efficiency is not the major concern for this project but the dumping of the unwanted power must be controllable.

![Figure 5-6](image_url)

**Figure 5-6** The input current increases as the effective resistance of the circuit decreases. The experimental result agrees with the theoretical estimation.

The boost converter was designed to regulate the excess current or the current caused by the thermal variation in the binary resistor network by changing its effective resistance. In order to make an accurate current regulation, we must be able to control the effective resistance of
the boost converter precisely. The experimental result agrees with the theory. Although a small difference is observed that can be caused by the measurement error and the inefficiency of the circuit, it is acceptable since we can always change its duty factor to meet the desired value. The continuous control is the greatest benefit to have the boost converter. We are able to change the input current freely from 0 to 4.3A (Figure 5-6) with fixed input voltage by just changing the duty factor in this experiment.

![Image of graphs showing current ripple and inductance vs. duty factor](image-url)

**Figure 5-7** A big jump and fall are observed in input current ripple and inductance respectively, which are caused by the inductor saturation. Note the inductance drops dramatically when duty factor is larger than 80%.

The current ripple was measured in the input, which has an increasing trend as we predicted in Figure 5-7a. However the input current ripple suddenly goes up when the duty factor goes beyond a certain point, which is caused by the inductor saturation. This phenomenon will significantly decrease the inductance of a ferrite-core inductor. We measured the slope of the input current ripple, input voltage and duty cycle to calculate the inductance using the equation $V = \frac{Ldi}{dt} / D$. In Figure 5-7b, the inductance drops from 5mH to less than 0.1mH, this rapid drop of inductance leads to 500% increase in the current ripple. According to Figure 5-6a and Figure 5-7b, the saturation current is about 1.5A, which is 50% smaller than the estimation. This can be caused by an incorrect relative permeability for the ferrite used, which indicates its real value is smaller.

We upgraded the boost converter with an extra feedback loop using one of the error amplifiers in TL494 to reduce the 100Hz ripple that is produced by the rectifier circuit in the power supply. This method reduced the current ripple very effectively. As shown in Figure 5-8, the input current ripple decreases as $R_f$ increases the open loop gain of the feedback system. For
example, when \( R_F \) is 10k\( \Omega \), the input current ripple is approximately 10 times smaller than the input current ripple without the feedback loop, which agrees with the theory. For better ripple reduction, a large \( R_F \) such as 100k\( \Omega \) should be used.

![Input Current Ripple Without Feedback Loop](image)

**Figure 5-8 Input current with and without the feedback loop. The amplitude of the ripple is decreased significantly with large \( R_F \).**

### 5.4 Conclusions

The experiment demonstrated the capacity of the boost converter to regulate current. The results are consistent with the theory. The primary goal was reached, we were able to control the input current with a fixed input voltage by varying the duty factor. The 100Hz current ripple from the main was very much reduced, which will be applied to the future full-scale model not only to reduce the ripple but also the thermal drift ripple due to temperature change.
Chapter 6

Full Scale PWM Current Converter Design

6.1 Introduction
The PWM (pulse-width modulation) boost converter is used to fill current gaps in the binary resistor network and to regulate against the effects of thermal drift. The boost converter should be able to regulate excess current that is equal to the maximum current gap of 21A in the proposed binary resistor network in chapter 3. However, to provide a margin of operation and to allow future higher rating applications, the boost converter was designed to have the current rating of 40A. The design will start with the diode and FET with high ratings to understand the behaviour of the circuit. Expensive IGBT modules that have built-in diodes were tested afterwards.

6.2 Boost Converter Module Selection
The most economical Semikron FET was not available in time, and even when it arrived, required a special printed circuit board connection. Therefore we used a FET and a diode with high current ratings to begin with. The characteristics of the first prototype boost converter
using a separate FET and diode are summarized in Table 6-1. After understanding the circuit behaviour at high current, we moved onto FET and IGBT modules, which are specialised in making boost converters. Their characteristics are summarized in Table 6-2, which were obtained using the online estimator provided by the manufacturer [13].

<table>
<thead>
<tr>
<th>STE180NE10_FET &amp; STPS160H100TV_DIODE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fsw (Hz)</strong></td>
</tr>
<tr>
<td>20k</td>
</tr>
<tr>
<td>20k</td>
</tr>
<tr>
<td>20k</td>
</tr>
</tbody>
</table>

Table 6-1 Performance description of FET - STE180NE10 and Diode – STPS160H100TV.

### 6.3 Experiment Setup

#### 6.3.1 Inductor design

As we have seen in chapter 5, the dramatic decrease in inductance due to the saturation of the ferromagnetic core caused large input current ripple. Therefore the inductor is preferably to be air-cored to prevent inductor saturation in the full-scale version of the boost converter. However, the inductor must have more turns to achieve a given inductance value without a high permeability core, and this will increase the cost because more copper is required. To minimize costs, the inductor was designed based on Brooks Ratio [10], which gives the maximum inductance with a given length of the copper wire.

![Figure 6-1 Schematic diagram showing the optimum shape for a multi-layer coil, created by R. Clarke, University of Surrey.](image)

Figure 6-1 Schematic diagram showing the optimum shape for a multi-layer coil, created by R. Clarke, University of Surrey.
<table>
<thead>
<tr>
<th>Fsw (Hz)</th>
<th>Rd</th>
<th>Vin (V)</th>
<th>Iin (A)</th>
<th>DF</th>
<th>Vout (V)</th>
<th>Iout (A)</th>
<th>P_fet_cond (W)</th>
<th>P_fet_tr (W)</th>
<th>P_fet (W)</th>
<th>P_diode (W)</th>
<th>T_fet (°C)</th>
<th>T_diode (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>250</td>
<td>10</td>
<td>3.6</td>
<td>99</td>
<td></td>
<td>0.928</td>
<td>50</td>
<td>6</td>
<td>20</td>
<td>33</td>
<td>53</td>
<td>9</td>
<td>98</td>
</tr>
<tr>
<td>25k</td>
<td>10</td>
<td>3.6</td>
<td>8</td>
<td>0.05 max</td>
<td>6</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>5</td>
<td>34</td>
<td>36</td>
<td>36</td>
</tr>
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<td>21</td>
<td>50</td>
<td>71</td>
<td>11</td>
<td>120</td>
<td>94</td>
</tr>
</tbody>
</table>

**MOSFET SK260MB10**

Table 6-2 Performance description of FET module and IGBT module.
Three coils in their cross section views are shown in Figure 6-1. They are made by the same length of copper wires but in different coil diameters. The inductance is linearly proportional to the coil diameter, therefore if a large inductance is required, a large diameter is required and the turns should be placed tightly to each other, the coil in Figure 6-1 satisfies the requirement. However, the number of turns is reduced by making the diameter large. On the other hand, the inductance increases with \( N^2 \) so the coil depicted on the left will not have a big inductance. The coil on the right in Figure 6-1 has a large number of turns but the diameter of each turn is small, especially to those near the centre of the coil that leads to a small inductance per turn. Also, the cross-sectional area of the coil is large, which leads to weak coupling between turns and lower flux linkage, particularly to those in the edge. The optimum ratio was calculated by Brooks in 1931, \( a = b = 3c / 2 \). The optimum shape is donut like but it is very hard to wind. Fortunately, the Brooks ratio is not critical, the ratio can deviate quite significantly before the inductance of the coil decreases very much [10]. The inductance of an inductor made in Brooks’ ratio is:

\[
L = 1.6994 \times 10^{-6} aN^2 \text{ (H)}
\]  

(6.1)

Since the boost converter works at low input voltage (\( \geq 3.6\text{V} \)), we must be careful with the voltage drop across the inductor because the collector-emitter voltage drop in IGBT can be significantly large, for example \( V_{\text{CE}} \) can be as high as 2.45V when collector current is 75A and \( V_{\text{GE}} \) is 15V. If the voltage-drop across the inductor is more than 1.15V, the IGBT cannot operate. Therefore the wire should have a large cross-section area to minimize the resistance as well as satisfying the current rating requirement. The minimum possible input voltage is when there is minimum current flowing through the Helical winding. The designed binary resistor network in chapter 3 can control the current in the Helical winding down to around 400A, this gives the minimum voltage of \( V_{\text{min}} = 400\text{A} \times 2.4\Omega = 0.96\text{V} \), which is a significantly small value and is already smaller than the minimum saturation voltage in IGBT. That is one of the reasons why IGBT will only be used in (future) high voltage applications. Fortunately, the voltage drop is usually small in FETs and when the input voltage is small, the gap between adjacent currents of the shunt network is smaller too but we still hope the voltage across the inductor can be less than 0.2V. The current rating of the wire is important but the large cross-section area that minimizes the stray resistance always leads to a higher current rating than we need.
A 4mH inductor that satisfies all conditions described above is very expensive to make. The cross-sectional area of the wire is at least 100 $mm^2$, and about 60 Kg of copper would be needed. Unfortunately, we were not able to make this inductor due to both time and budget constraints. Specifically, there was a problem with ringing at 7MHz in the first prototype inductor which matched its measured self-resonant frequency. It was judged that investing the time effort into making a 100A rated inductor was not justifiable until the self-resonance problems were better understood. Therefore we found a substitute, using some existing wire with a cross-section area of about 25 $mm^2$ and a 4 $mm$ thick, low dielectric constant insulation with a length of about 100m found in the basement of the Research School of Physical Science and Engineering. We hand wound the wire onto a wooden core, and carefully layered the winding, both measures aim at reducing stray capacitance. This inductor has a current rating of at least 50 A and an inductance of 1.25 mH and a stray capacitance of 220 pF. This was adequate for prototyping purpose, and would provide data on the importance of stray capacitance, and cooling considerations. A photo of the inductor is in Appendix A.

### 6.3.2 Drivers and Voltage/Current Protections

The switching devices is controlled by SEMIDRIVER SKHI22A, which is a hybrid timing controller and power driver circuit specially designed to drive and protect up to two FET-type switching devices at the same time. The driver requires logic input signals that will be generated by TL494, the same device used in the small-scale boost converter. The SKHI22A shapes the signal pulses coming from the TL494 to make the smaller rise/fall time possible, and to avoid incorrect drive pulse shapes and sequences. The chip has a built-in $V_{CE}$ or $V_{DS}$ ($V_{CE}$ for IGBT and $V_{DS}$ for FET, $V_{CE}$ will be used from now on for easier reading) monitor that shuts down the switching device when an incomplete turn-on is detected. In other words, if $V_{CE}$ is still higher than the reference voltage at a certain time delay after turn-on, the chip will shut down the switching device, which provides an ideal over-current or under-drive protection.

Semiconductor switches such as FET and IGBT have absolute voltage ratings. However, in this type of circuit, they are most likely to be stressed beyond ratings at full power operations when duty factor is large. For example,

\[ V_{in} = (1 - D_1) V_{out1} \]  \hspace{1cm} (6.2)

\[ V_{in} = (1 - D_2) V_{out2} \]  \hspace{1cm} (6.3)
Assuming $V_{out2} = 2V_{out1}$

Substitute equation (6.3) to equation (6.2) and rearrange, we have:

$$1 = 2D_2 - D_1$$

(6.4)

Therefore when $D_1 = 90\%$, $D_2 = 95\%$.

From the above calculation, the output voltage is doubled with only 5\% change in duty factor, which is a potential risk of destroying semiconductor devices. Therefore a reliable over-voltage protection is required.

The chip was designed to detect a fault and safely shut down all switching signals if there is an excessive voltage when the switching device is turned on (i.e. an incomplete turn-on). Because the incomplete turn-on monitor for each channel only operates when the device is intended to be turned on, we apply signals to the channel 2 input as if it were being driven when the actual device (fed by channel 1) is off. In this way, if we feed such a complementary signal to channel 2, the channel 2 $V_{CE}$ monitor can be used to detect over-voltages in the off-state for the switch device in the first channel. In other words, the chip “thinks” the secondary switching device is experiencing an over-voltage and will stop operating both channels even though only one switching device exists. The built-in error amplifier in TL494 can be used for over-current protection and current ripple reduction. Please refer to chapter 5 for details.

6.3.3 Other Components

The output filter capacitor is 10 mF. The capacitance value does not have to be so large but the capacitor with this capacitance value has good tolerance to AC current up to 15A RMS in the frequency range, which could cause heating by dissipation in the internal stray resistance. This large value slows the response of the PWM circuit to changes in duty factor, and must be considered when implementing feedback control.

The design of a RC snubber circuit was based on the theory mentioned in section 2.3.2. The stray inductance was estimated to be about 500 nH and the RC values were calculated to be $2\Omega$ and 68 nF respectively. There are two important stray inductances, both are important because they are in parts of the circuit where there is a large di/dt, FET switch and the loop of the flywheel diode and the output capacitor loop. Both have to be considered, but because the FET is compact and the RC snubber is very close to it, the stray inductance there is quite
small. The loop of the flywheel diode and the output capacitor is the biggest, which is why we concentrated on it. The $R_o$ resistor is not as important as the capacitor shunts most of the current on faster timescales.

The heat sink is designed to absorb the heat generated by semiconductor devices under worst-case conditions, and is rated at 100 W.

### 6.4 Full Scale Boost Converter using STPS160H100TV and STE180NE10

The voltage across FET, $V_{DS}$, was monitored carefully when we increased the duty cycle and input voltage. A voltage spike is observed during the turn-off transient at high duty cycle (Figure 6-2). The RC snubber did not reduce the ringing effectively. We tried to reduce the amplitude of the voltage spike by reducing the snubber resistance but as the resistance was reduced, the stray inductance became under-damped, which made $V_{DS}$ to ring more and became unstable during the turn-off.

![LTSpice simulation with RC Snubber](image1)

![LTSpice simulation with RCD and RC Snubber](image2)

Figure 6-2 Measured FET Switching transients at DF = 91.5% are shown in the right. The voltage spike reaches 70 V when only the RC snubber is used. The voltage $V_{DS}$ is clamped to 45 V with the presence of RCD snubber. The blue line indicates the power dissipation. The simulated transient response with RC snubber and RCD snubber are shown in the left. Note the peak voltage is reduced significantly with an additional RCD snubber. Note that there exists a constant scaling factor between the simulations and the experimental results.
We introduced another snubber to clamp the voltage known as a voltage clamp RCD snubber[7][8][9]. The snubber has three components, a resistor, a capacitor and a diode. This kind of snubber is not good at damping because the diode makes the RCD snubber polarized and therefore it is mostly not active during cycles since the diode only allows current to flow in a single direction.

Similar to ordinary RC snubber that was explained in chapter 2, its RC values set the clamped voltage, which was chosen to be about 50 V, twice smaller than the absolute voltage rating to ensure FET is safe since there might be some harmful high frequency components that cannot be detected. The current rating of the current controller is 40 A and makes the snubber resistance to be around 1Ω. We examined the ringing and found it rings at 8 MHz. We suspected it can be the resonance frequency between the output capacitance of the FET and the stray inductance within the circuit. The output capacitance is 2.2 nF [14]. The LC resonance equation was used to find out its stray inductance:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

The stray inductance was calculated to be 180 nH. By using equation (2.17), the snubber capacitance was calculated to be 45 nF. A fast Schottky Diode should be used to ensure a fast response to the transients.

We used LTSpice to model the transients. The stray inductances are allocated in the circuit and the real Spice components that downloaded from manufacturer are used (Figure 6-3). A similar voltage spike at the FET drain is observed when the ordinary RC snubber is used only. The RCD snubber is then introduced to the circuit simulation and the voltage spike is found to be significantly reduced (Figure 6-2).

![Figure 6-3 LTSpice Simulation. RCD and RC snubbers are used in this model. The capacitance in RCD snubber is larger than the calculated value because in the real circuit, we use two RCD snubbers in parallel with the same rating for the maximum FET safety.](image-url)
We then introduced the RCD voltage clamp snubber to the real circuit. The voltage spike in the FET drain voltage turn-off transients is clamped (Figure 6-2) and have a good agreement with the LTSpice simulation. In addition, $V_{DS}$ would ring badly if there was only RCD snubber in the circuit because the RCD snubber cannot over-damp the large stray inductance from other part of the circuit efficiently due to its small snubber resistance, the RC snubber that has greater snubber resistance is still required (Figure 2-6).

The switching losses were measured, which were 3.1 W and 3.5 W for RC snubber only and both RC and RCD snubbers respectively. The additional RCD snubber seems to increase the power dissipation in the FET slightly because the snubber diode decreases the power dissipation in the snubber resistor and the FET has to dissipate this power. However it is tolerable since the maximum power rating for this FET is over 300W [14] and the voltage is the primary concern here.

The conduction loss was 2.5 W at duty cycle of 91.5%, which is quite small because the drain-source on resistance is small in FET, which is $4.5 \, m\Omega$. We did not measure the power dissipation in diode because it was too tricky to measure the voltage drop and current with the presence of the RC snubber across the diode. Since it is a Schottky diode, it should not dissipate too much heat. The most power is dissipated in the inductor as shown in Figure 6-4. It dissipates almost 40 W at 91.5 % duty cycle. The only way to reduce power dissipation of the inductor in our project is to use an inductor wound using larger diameter copper wire to reduce the stray resistance.

Figure 6-4 Power dissipation in the inductor. The power dissipation is almost 40W at the duty cycle of 91.5%.
The output voltage response and the efficiency are plotted in Figure 6-5. The output voltage has the same trend to theoretical value but the difference gets larger at high duty cycle because the parasitic elements dissipate power, especially the parasitic resistance in the inductor that dissipates almost 40 W at the highest duty cycle. This leads to a low efficiency when the duty cycle is close to one.

We are able to control the input current from 0 to 25A by changing the duty cycle from 0 to 91.5% (Figure 6-6). The experimental values agree with the theory. We could not perform experiment for higher duty cycle. The combination of the TL494 and the minimum pulse width requirement of the SKI22 restricts the maximum duty cycle. Also, the requirement that complementary pulses applied to the SKI22 not overlap requires a clear margin of 3.3 μs that further limits the duty cycle.
The input current ripple was measured, and is slightly larger than the theoretical values. This can be caused by an over-estimated inductance and bad measurement, the waveform is fuzzy, and is very difficult to tell the actual upper and lower voltage boundaries. The only way to reduce the ripple is to use an inductor with higher inductance.

![Theoretical Value](image)

**Figure 6-7** The input current ripple.

### 6.5 Full Scale Boost Converter using SKM100GB173D

The IGBT was used in this experiment. Since the IGBT has a high $V_{CE}$ drop, at least 1.5 V when $I_C$ is 40 A and there is another 1.5 V drop in the inductor, tests were performed with an increased the input voltage of 7 V compared to 3.6 V so that the current levels were comparable to those in the FET tests. Unfortunately, this causes the power dissipations of the FET and the IGBT to be incomparable.

![Transient Response](image)

**Figure 6-8** The transient response of the IGBT without any snubber protection is shown in the left. The transient response when RCD snubbers are installed is shown in the right. The blue line indicates the power dissipation.
The IGBT has a voltage rating of 1700 V, which is significantly larger than our requirement. It should be able to switch safely without the snubber circuit. $V_{CE}$ was measured without the presence of snubbers, and a large voltage spike of 125 V is observed (Figure 6-8). Although it is small compared to its voltage rating, snubbers were still used to protect it. The RCD snubber circuits from FET were used again, which reduced the voltage spike down to 70 V (Figure 6-8). The switching losses were measured, which were 3.2 W and 5.5 W for RC snubber only and both RC and RCD snubbers respectively.

**Figure 6-9** The output voltage and the efficiency.

The output voltage response and the efficiency are plotted in Figure 6-9. The output voltage has the same trend to theoretical value but the difference gets larger at high duty cycle, the output voltage starts to increase very slowly when duty cycle reaches 90%. The voltage drop in the inductor could be responsible for this discrepancy. This leads to a low efficiency when the duty cycle is close to one.

**Figure 6-10** The input current increases as the effective resistance of the circuit decreases. The experimental result agrees with the theoretical estimation.
We are able to control the input current from 0 to 30A by changing the duty cycle from 0 to 91.5% that makes a good agreement with the theory (Figure 6-10).

The experimental input current ripple agrees with the theory (Figure 6-11). The only way to decrease the ripple is to increase the inductance of the inductor.

![Input Current Ripple](image)

**Figure 6-11 The input current ripple.**

### 6.6 Labview Computer Control

The PWM current controller or the boost converter can be controlled by a computer via LabVIEW interface. We designed a LabVIEW program, which can adjust the current automatically. When a required current is entered into the program, LabVIEW will generate a voltage to drive the TL494 chip as the control signal to create a duty cycle. The real output current is detected by a current probe, the signal is transferred back to the program and is compared with the required current. If a difference is detected, LabVIEW will increase or decrease the control voltage to the TL494 until there is zero difference between the measured value and the required value. We have successfully control the current up to 30 A with 1 A step using a discrete-time proportional controller in LabVIEW.

### 6.7 Discussion

We have built two boost converters using two different switching devices (Appendix A). The results show a good agreement with the theory. The voltage spike caused by the output capacitance of the FET and the stray inductance was reduced significantly by introducing an additional RCD snubber circuit. The voltage spike was reduced by 50%. The current ripple was increased, which we expected. The current ripple can be reduced by using an inductor
with higher inductance. The over-voltage protection kicked in when the output voltage was higher than the threshold but we still had to be careful, there were no significant voltage spikes that were too short to be properly resolved, and that may destroy the FET. Although IGBT has a voltage rating significantly higher than our low voltage application, a voltage clamp snubber was still used to protect it. This is a good practice for IGBT high voltage applications in the future. The inductor design is more difficult and complicated than we expected. Although the current inductor is sufficient for prototyping purpose, a better one will be required in the final product.
Chapter 7

Conclusions and Future Plans

7.1 Conclusions

We designed and tested a precision high current controller comprising a binary resistor network capable of dissipating 828 W and an electronically controllable pulsed width modulated fine controller capable of currents up to 30 A.

A binary resistor network that consists of nine binary branches was designed to achieve a wide range of current regulation from 420 A to 1500 A and a maximum adjacent current gap of 21 A. Although only four binary branches were assembled due to safety and time constraints, the experimental results show good agreement with theory. The binary resistor network is LabVIEW computer-controlled and its effective resistance is less than 3% different from the requirement.

We have both theoretically and experimentally investigated the PWM current converter. A small-scale prototype PWM converter was built first to prove the theory, and it was able to
control the input currents up to 4.3 A. We also minimized the 100 Hz ripple coming from the power supply by introducing a feedback loop control using the TL494 PWM controller. The amplitude of the ripple was reduced from 3 mA to less than 0.2 mA.

Two large-scale LabVIEW computer controlled PWM controllers were built using two switching devices after successfully tests of the small-scale one. The results were consistent with the theory. We are able to control the input currents up to 25 A using a power FET at an input voltage of 3.6 V and 30 A, using an IGBT at an input voltage of 7 V. An over-voltage protection was developed to avoid destroying the solid state switches. We studied the transient response of the switches and determined that the occurrence of a large voltage spike at the FET turn-off is caused by the resonance between the stray inductance within the circuit and the output capacitance of the switch. A simple RC snubber was not sufficient to suppress the spike, therefore we introduced an RCD voltage clamp snubber to very effectively reduce the voltage spike.

A temporary inductor was used for the full-scale PWM current controller prototype. The inductance was not large enough to minimize the input current ripple but it was reasonable for the prototyping purpose. The low input voltage to the PWM current controller was identified as an important issue. The cross-sectional area of the copper wire that is used to make the inductor is large enough to carry the current but it is not large enough to minimize the stray resistance to reduce the voltage drop across the inductor. The voltage drop for the temporary inductor is 1.65 V at 25 A. It is acceptable for the PWM converter using the FET but it is not low enough for the IGBT because IGBT has a greater voltage drop of 1.5 V which in conjunction with the voltage drop across the inductor make the operation marginal at best.
7.2 Future Plans

There are some issues about the inductor that can be improved:

- Voltage drop.
- Cooling, it is less of an issue if the voltage drop problem is solved.
- Inductance, a high inductance inductor can keep the 20 kHz ripple low.
- Stray capacitance, there are two impacts:
  
  I. It produces ringing at the terminals of the switching device which may damage it.
  
  II. Although 220 pF seems low compared to $C_{DS}$, such a capacitance can conduct switching transients in the range ~ MHz back into input circuit (e.g. Helical winding).

Therefore a better inductor will be designed and built using the understanding gained in reducing stray capacitance and ripple to minimize the stray resistance for the final product when copper of the required rectangular cross section can be procured.

We also will study the effectiveness of cooling. Squirrel cage blowers will be installed to the system if natural cooling is not effective enough.

The main goal for this project was to develop a controllable precision current shunt suitable for operation with the Helical winding of the H-1 Heliac. A secondary goal was to explore extending the operational range of the circuit to allow limited control of the main windings (~20-50 mΩ) at currents up to 7000 A for short pulses up to 3 seconds. This implies an operational voltage of 140-350 V, which requires a much higher voltage rating for the switching device. As initial (low voltage) tests using an IGBT rated at up to 1700 V were successful, we will construct a separate PWM circuit, using the same driving and control electronics for such operation, and apply feedback control to attempt to reduce the residual 30 Hz ripple in the H-1 power supply.
References


Appendix A

The full-scale PWM current converter:
Appendix B

The process of making a hand-wound inductor, from left to right: Greg, Mark, Tony, and Horst.

Boyd and Tony.

John is fixing contactors onto the MDF.